PXIe-5450 Specifications

2023-08-09

Contents

PXIe-5450 Specifications

These specifications apply to the 128 MB and 512 MBPXIe-5450.

> **Caution** The outputs of this sensitive test and measurement product are not protected for electromagnetic interference for functional reasons. As a result, this product may experience reduced accuracy or other temporary performance degradation when cables are attached in an environment with electromagnetic interference present.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Signals terminated with 50 Ω to ground
- Direct path set to 0.5 V_{pk} differential (gain = 0.5, 1 V_{pk-pk} differential)
- Sample clock set to 400 MS/s
- Onboard Sample clock with no Reference clock

- 0 °C to 55 °C ambient temperature

Warranted specifications are valid under the following conditions unless otherwise noted.

- 15 minutes warm-up time at ambient temperature
- Calibration cycle maintained
- Chassis fan speed set to High
- NI-FGEN instrument driver used
- NI-FGEN instrument driver self-calibration performed after instrument is stable

Typical specifications are valid under the following conditions unless otherwise noted:

- Over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production

Analog Outputs

CH 0+/–, CH 1+/– (Analog Outputs, Front Panel Connectors)

Number of channels	2
Output type	Differential
Output paths	Direct path
DAC resolution	16 bits

Amplitude and Offset

Amplitude resolution	4 digits, <0.0025% (0.0002 dB of amplitude range)

Table 1. Differential Full Scale Amplitude Range

Flatness Correction State	Load	Amplitude (V_{pk-pk})	
		Minimum Value	Maximum Value
Disabled	50 Ω	0.708	1.00
	1 kΩ	1.35	1.90
	Open	1.42	2.00
Enabled	50 Ω	0.567	0.8
	1 kΩ	1.08	1.52
	Open	1.14	1.6

Accuracy

Accuracy

DC Accuracy Measured with a DMM. Differential offset is not adjusted during self-calibration. Measured with both output terminals terminated to ground through a high impedance.

Absolute gain error	
Within ±5 °C of Self-Cal temperature	±0.2% of differential output range
Outside ±5 °C of Self-Cal temperature	+ 0.030%/°C + 0.015%/°C, typical

Absolute Differential Offset	±1 mV (0 °C to 55 °C)
Absolute common mode offset	±350 µV (0 °C to 55 °C)
Channel-to-channel relative gain error	
Within ±5 °C of Self-Cal temperature	±0.08% of differential output range
Outside ±5 °C of Self-Cal temperature	+ 0.010%/°C + 0.005%/°C, typical

AC Amplitude Accuracy Measured using a DMM, with full-scale data into highimpedance, 50 kHz sine wave, 400 MS/s.

Absolute AC amplitude accuracy	
within ±5 °C of Self-Cal temperature	±0.5% of differential output range
Channel-to-Channel, relative AC amplitude accuracy	
within ±5 °C of Self-Cal temperature	±0.2% of differential output range ±0.07% of differential output range, typical
Channel-to-channel timing alignment accuracy	35 ps 25 ps, typical

Output Characteristics

Output impedance	50 Ω nominal, per connector
Return loss (differential), nominal	

Single-ended direct path	
5 MHz to 60 MHz	26 dB
60 MHz to 145 MHz	15 dB
Differential direct path	
Up to 20 MHz	35 dB
Up to 60 MHz	22 dB
Up to 145 MHz	12 dB
Load impedance compensation	Output amplitude is compensated for user-specified load impedance to ground. Performed in software.
Output coupling	DC
Output enable	Software-selectable. When disabled, output is terminated with a 50 Ω, 1 W resistor.
Maximum output overload	±8 V from a 50 Ω source
Waveform summing	The output terminals support waveform summing, which means the outputs of multiple PXIe-5450 signal generators can be connected together.

Frequency Response

Analog bandwidth, typical	
Baseband	145 MHz for each I and Q output

Complex baseband	290 MHz when used with external I/Q modulator
Analog filter	4-pole filter for image suppression

Table 2. Passband Flatness

Passband Flatness	Flatness Correction Disabled	Flatness Correction Enabled
0 MHz to 60 MHz	0.5 dB, typical	0.24 dB 0.13 dB, typical
60 MHz to 120 MHz	1.9 dB, typical	0.34 dB 0.19 dB, typical

Table 3. Passband Flatness

Passband Flatness	Flatness Correction Disabled	Flatness Correction Enabled
Channel-to-Channel Passband Flatness Matching 0 MHz to 60 MHz	0.05 dB, typical	0.03 dB, typical
Channel-to-Channel Passband Flatness Matching 60 MHz to 120 MHz	0.18 dB, typical	0.04 dB, typical

Figure 1. Amplitude Response with Flatness Correction Enabled, 400 MS/s, Differential, Referenced to 50 kHz, Typical

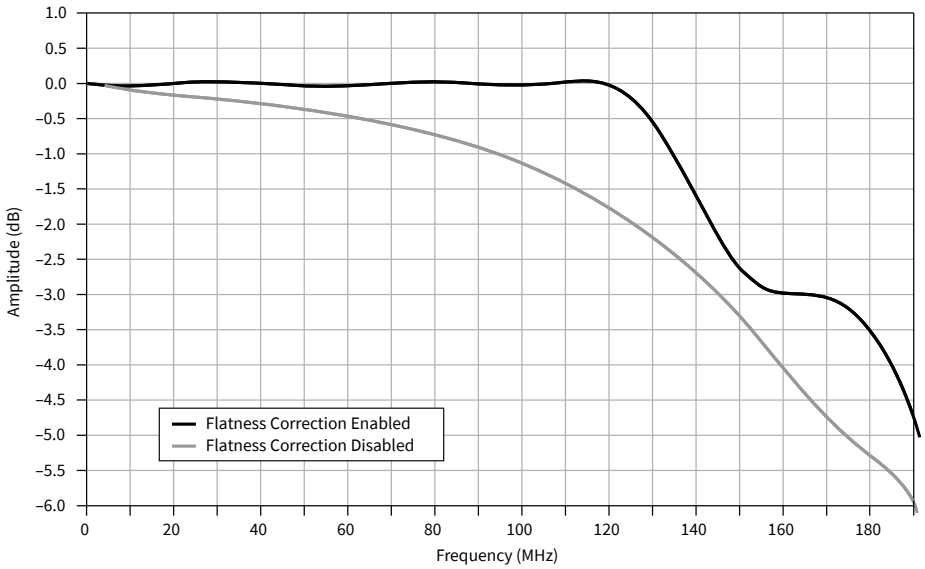


Figure 2. Amplitude Response, Flatness Correction Enabled, 400 MS/s, Differential, Referenced to 50 kHz, Typical

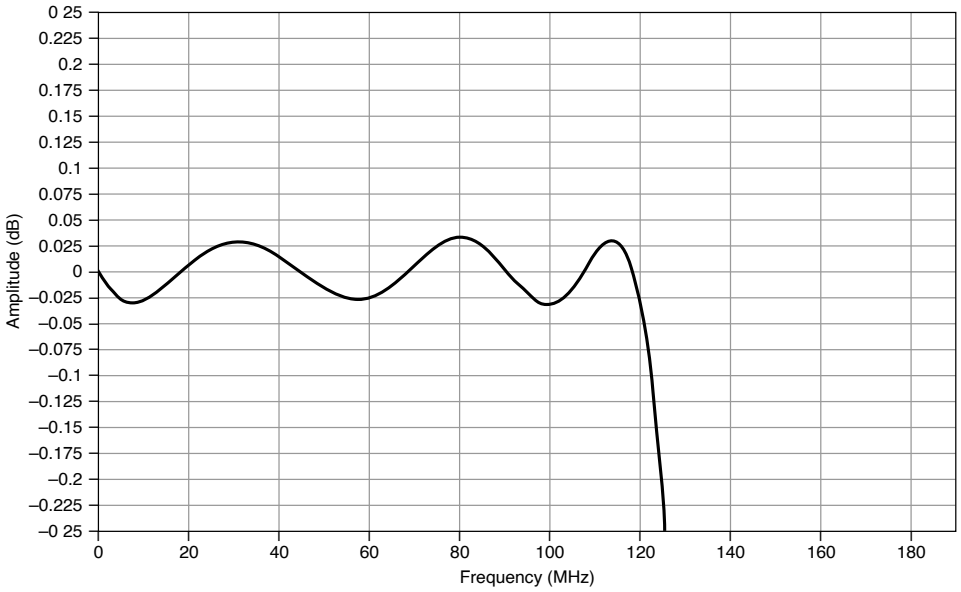
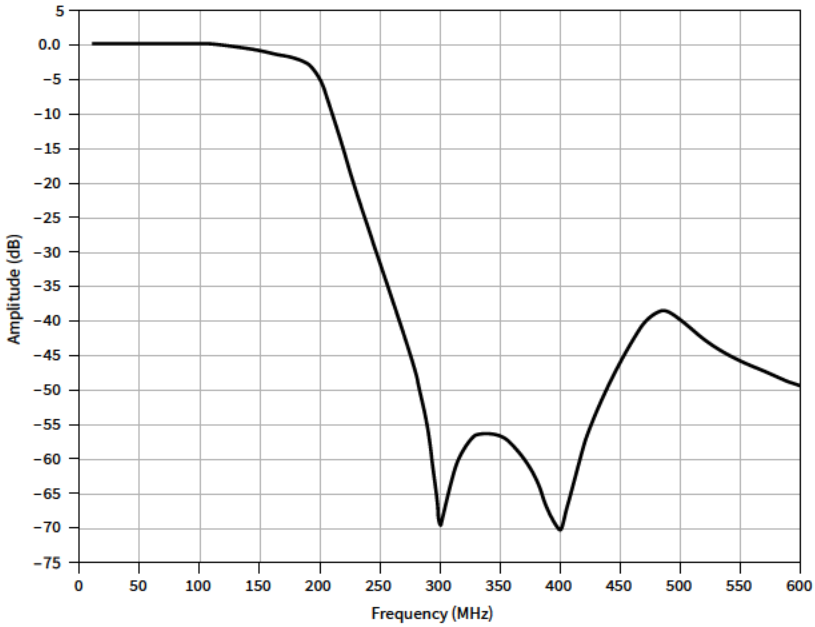


Figure 3. Characteristic Frequency Response of Image Suppression Filter, Typical



Note Sinc response due to DAC sampling is not included in the previous figure.

Spectral Characteristics

Table 4. Nominal Spurious Free Dynamic Range (SFDR) at 1 MHz

Frequency Range	SFDR Without Harmonics (dB)	SFDR With Harmonics (dB)
DC to 7 MHz	98	88
DC to 200 MHz	84	75

Table 5. SFDR with Harmonics

Frequency (MHz)	SFDR (dB)
10	70 (74)
60	68 (70)
100	62
120	62

Frequency (MHz)	SFDR (dB)
160	62

Table 6. SFDR without Harmonics

Frequency (MHz)	SFDR (dB)
10	70 (74)
60	68 (73)
100	64
120	62
160	62

Table 7. Out-of-Band Performance, Nominal

In-Band Tone Frequency (MHz)	Out of Band Spur Level (dBm)
0 to 20	<–80 dBm
20 to 50	<–65 dBm
Channel-to-Channel Crosstalk	
0 MHz to 200 MHz	<80 dBc, nominal
0 MHz to 150 MHz	<90 dBc, nominal

Table 8. Total Harmonic Distortion (THD), Typical

Frequency (MHz)	THD (dBc)
10	-75
20	-70
40	-68
80	-68
100	-68
120	-78
160	-83

Table 9. Intermodulation Distortion (IMD_3), Typical

Frequency (MHz)	IMD (dBc)
10	-84
20	-81
40	-75
80	-71
100	-68
120	-68
160	-66

Table 10. Average Noise Density

Amplitude Range		Average Noise Density		
V_{pk-pk}	dBm	Object Missing This object is not available in the repository.	dBm/Hz	dBFS/Hz
1	4.0	2.24	-160	-164

Figure 4. Total Harmonic Distortion, Typical

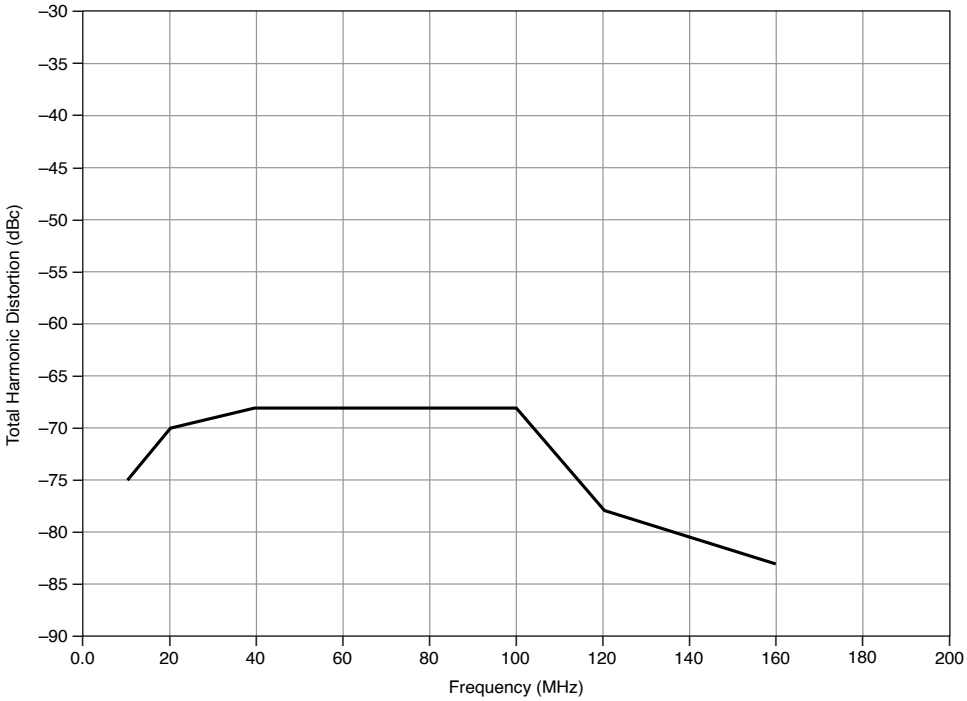


Figure 5. Intermodulation Distortion, 200 kHz Separation, Typical

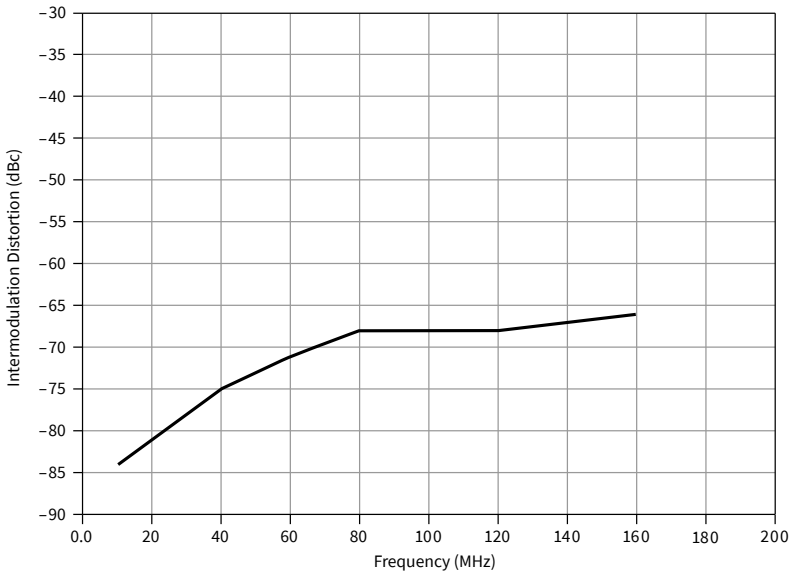


Figure 6. Intermodulation Distortion, 1 MHz Separation, 20 MHz Tone, 400 MS/s, – 7 dBFS, Typical

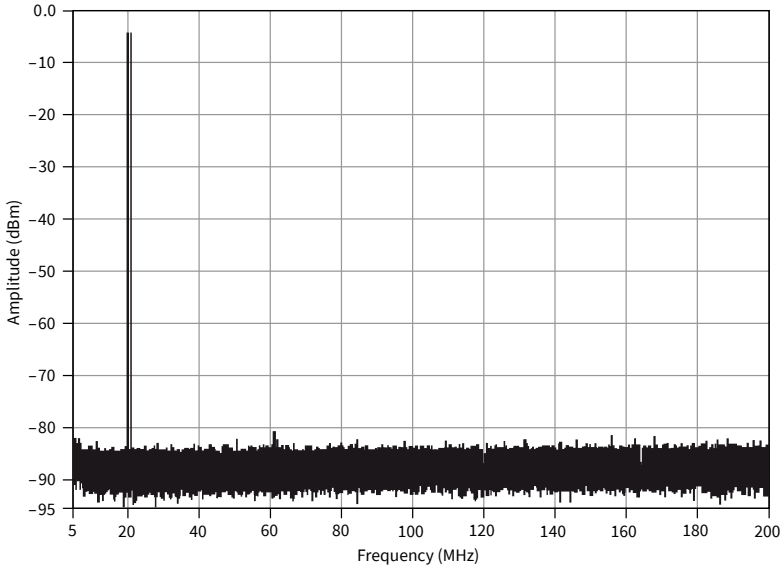


Figure 7. 10.000 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Typical

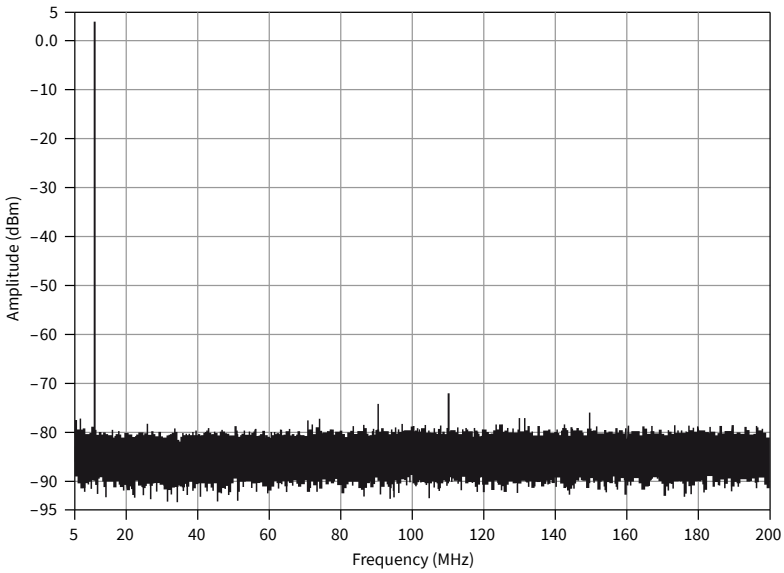
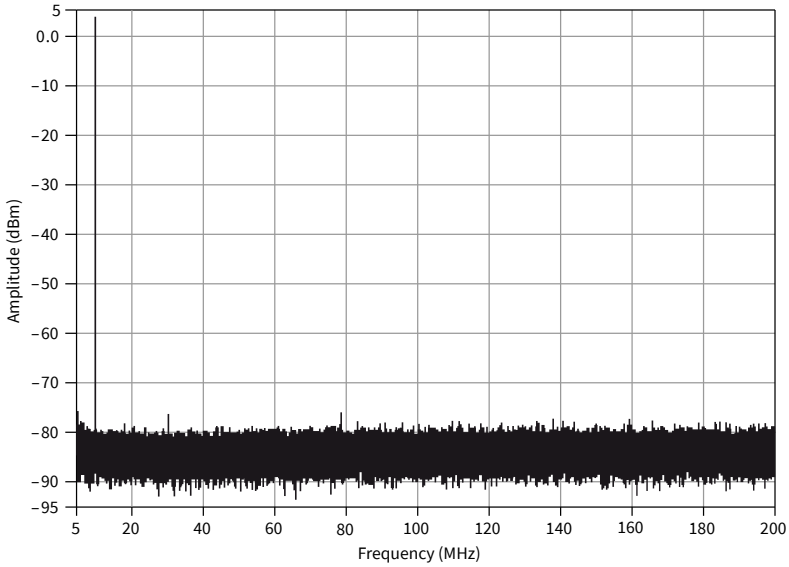


Figure 8. 10.100 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Typical



Output Phase Noise and Jitter

Table 11. Output Phase Noise and Jitter, Typical

Sample Clock Source	Output Freq. (MHz)	System Phase Noise Density (dBc/Hz)					System Output Integrated Jitter
		100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	
Internal, High Resolution Clock, 400 MS/s	10	<-121	<-137	<-146	<-152	<-153	<350 fs
	100	<-101	<-119	<-126	<-136	<-141	<350 fs
CLK IN External 10 MHz Reference Clock,400 MS/s	10	<-122	<-135	<-146	<-152	<-153	<350 fs
	100	<-105	<-115	<-126	<-136	<-141	<350 fs

Figure 9. Phase Noise on a Representative Module, 100 MHz Sine Wave, 400 MS/s Internal Clock Sample Rate, Chassis Fans Low, Shown With and Without a Reference Clock

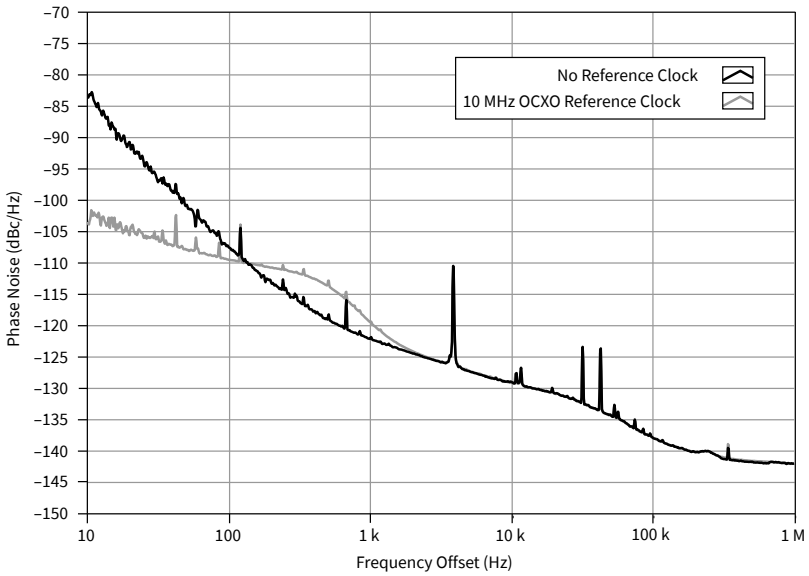
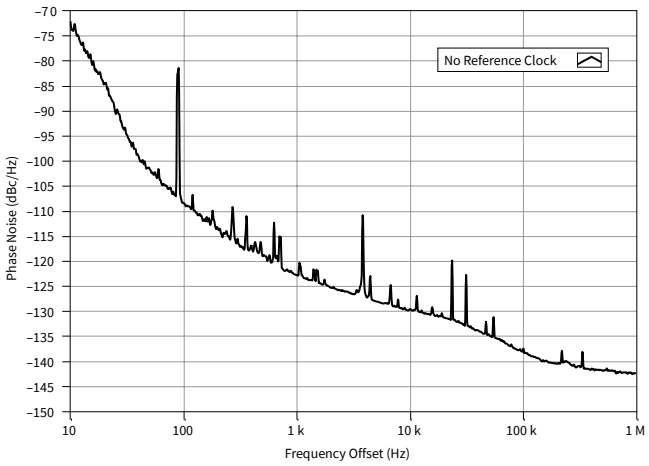


Figure 10. Phase Noise on a Representative Module, 100 MHz Sine Wave, 400 MS/s Internal Clock Sample Rate, Chassis Fans High, No Reference Clock



Suggested Maximum Frequencies for Common Functions

Sine	145 MHz
Square	33 MHz(<133 V/µs slew rate)

Ramp	1 MHz(<50 V/µs slew rate)
Triangle	8 MHz

Pulse Response, Typical

Typical Rise/Fall Time (10% to 90%)	
Flatness correction disabled	3 ns
Flatness correction enabled	2.5 ns
Aberration	
Flatness correction disabled	18% (7%)
Flatness correction enabled	22%

Clocking

Onboard Sample Clock

Sample clock rate range	12.2 kS/s to 400 MS/s
Sample clock rate frequency resolution	<5.7 µHz
Sample clock delay	0 ns to 2 ns, independent per channel
Sample clock delay resolution	10 ps nominal
Sample clock timebase phase adjust	±1 Sample clock timebase period

Reference Clock Sources	None (internal reference)

	PXI_CLK10 (backplane) CLK IN (front panel connector)
Reference Clock Frequency	1 MHz to 100 MHz in increments of 1 MHz 100 MHz to 200 MHz in increments of 2 MHz 200 MHz to 400 MHz in increments of 4 MHz Default of 10 MHz
Internal Reference Clock Frequency Accuracy	±0.01%

External Sample Clock

External Sample clock source	CLK IN front panel connector, with multiplication and division
External Sample clock rate	10 MS/s, 20 MS/s to 400 MS/s
Sample Clock rate range	12.2 kS/s to 400 MS/s
Multiplication/Division factor range	Varies depending on the external Sample clock rate
External Sample clock delay	0 ns to 2 ns, independent per channel
External Sample clock delay resolution	10 ps, nominal
External Sample clock timebase phase adjust	±1 Sample clock timebase period

External Sample Clock Timebase

External Sample clock timebase sources	CLK IN front panel connector, with division
External Sample clock timebase rate range	200 MS/s to 400 MS/s
Divide factor range	1, 2 to 32768 in steps of 2
Sample Clock delay	0 ns to 2 ns, independent per channel
Sample Clock delay resolution	10 ps nominal

Exporting Clocks

Table 12. Exported Clock Rates

Clock	Destination	Rates
Reference Clock	CLK OUT	1 MHz to 400 MHz
	PFI<0..1>	1 MHz to 200 MHz
Sample Clock	CLK OUT	100 kHz to 400 MHz
	PFI<0..1>	0 MHz to 200 MHz
Sample Clock Timebase	CLK OUT	100 kHz to 400 MHz
	PFI<0..1>	0 MHz to 200 MHz

Terminals

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Direction	Input

Destinations	Reference clock, Sample clock, or Sample clock timebase
Frequency range	1 MHz to 400 MHz
Input impedance	50 Ω , nominal
Input voltage range	
50% duty cycle input	500 mVpk-pk to 5 Vpk-pk into 50 Ω (–2 dBm to +18 dBm)
45% to 55% duty cycle input	550 mVpk-pk to 4.5 Vpk-pk into 50 Ω (–1.2 dBm to +17 dBm)
Input protection range	
50% duty cycle input	6 V_{pk-pk} into 50 Ω (19.5 dBm)
45% to 55% duty cycle input	5.4 V_{pk-pk} into 50 Ω (18.5 dBm)
Duty cycle requirements	45% to 55%
Input coupling	AC
Voltage standing wave ratio (VSWR)	1.3:1 up to 2 GHz, nominal

CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)

Direction	Output
Sources	Sample clock, divided by integer K (1≤ K ≤ 3, minimum), Reference clock, or Sample

	clock timebase, divided by integer M (1 ≤ M ≤ 1048576)
Frequency Range	100 kHz to 400 MHz
Output Voltage	≥0.7 V_{pk-pk} into 50 Ω typical
Maximum Output Overload	3.3 V_{pk-pk} from a 50 Ω source
Output Coupling	AC
VSWR	1.3:1 up to 2 GHz nominal

PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Direction	Bidirectional
Frequency Range	DC to 200 MHz
As an Input (Trigger)	
Destinations	Start trigger, Script trigger
Input Range	0 V to 5 V
Input Protection Range	-2 V to +6.5 V
Input voltage	
V_{IH}	1.8 V
V_{IL}	1.5 V

Input Impedance	10 kΩ , nominal
As an Output (Event)	
Sources	Sample clock divided by integer K (2 ≤ K ≤ 3, minimum), Sample clock timebase divided by integer M (2 ≤ M ≤ 1048576), Reference clock, Marker event, Data marker event, Exported Start trigger, Exported Script trigger, Ready for Start event, Started event, or Done event
Output impedance	50 Ω , nominal
Maximum Output Overload	–2 V to +6.5 V
Output voltage	
Minimum V_{OH}	2.4 V (Open load) 1.3 V (50 Ω load)
Maximum V_{OL}	0.4 V (Open load) 0.2 V (50 Ω load)
Rise/Fall Time	3 ns, typical

Triggers and Events

Triggers

Sources	PFI<0..1> (SMB front panel connectors) PXI_Trig<0..7> (backplane connector) Immediate (does not wait for a trigger). Default.

Types	Start trigger edge, Script trigger edge and level, Software trigger
Edge detection	Rise, falling
Minimum pulse width	25 ns
Delay from trigger to analog output with OSP disabled	154 Sample clock timebase periods + 65 ns, nominal
Additional delay with OSP enabled	Varies with OSP configuration
Trigger exporting	
Exported Trigger Destinations	PFI<0..1> (SMB front panel connectors) or PXI_Trig<0..6> (backplane connector)
Exported Trigger Delay	50 ns, nominal
Exported Trigger Pulse Width	>150 ns

Events

Destinations	PFI<0..1> (SMB front panel connectors) PXI_Trig<0..6> (backplane connector)
Types	Marker<0..3>, Data Marker<0..1>, Ready for Start, Started, Done
Quantum	Marker position must be placed at an integer multiple of two samples.
Width	Adjustable, minimum of 2 samples. Default is 150 ns.

Skew, with respect to analog output	
PFI<0..1>	±3 Sample clock periods
PXI_Trig<0..6>	±6 Sample clock periods

Waveform Generation Capabilities

Memory Usage	The PXIe-5450 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.
Onboard Memory Size	
128 MB option	134,217,728 bytes
512 MB option	536,870,912 bytes
Loop Count	1 to 16,777,215 Burst trigger: Unlimited
Quantum	Waveform size must be an integer multiple of two samples.
Output modes	Arbitrary Waveform, Script, and Arbitrary Sequence

Table 13. Minimum Waveform Size (Samples)

Trigger Mode	Number of Channels	Arbitrary Waveform Mode	Arbitrary Sequence Mode >180 MS/s	Arbitrary Sequence Mode ≤180MS/s
Single	1	4	2	2
	2	4	4	4
Continuous	1	142	140	58
	2	284	280	116
Stepped	1	210	154	54
	2	420	308	108
Burst	1	142	1,134	476
	2	284	2,312	952

Table 14. Memory Limits (Bytes)

Generation Mode	Number of Channels	128 MB	512 MB
Arbitrary Waveform Mode, Maximum Waveform Memory	1	67,108,352	268,434,944
	2	33,553,920	134,217,216
Arbitrary Sequence Mode, Maximum Waveform Memory	1	67,108,352	268,434,944
	2	33,553,920	134,217,216
Arbitrary Sequence Mode, Maximum Waveforms	1	1,048,575	4,194,303
	2	524,287	2,097,151
Arbitrary Sequence Mode, Maximum	1	8,388,597	33,554,421
	2	4,194,293	16,777,205

Generation Mode	Number of Channels	128 MB	512 MB
Segments in a Sequence			

Table 15. Maximum Waveform Play Times

Sample Rate	Number of Channels	128 MB	512 MB
400 MS/s	1	0.17 seconds	0.67 seconds
	2	0.084 seconds	0.34 seconds
25 MS/s	1	2.68 seconds	10.74 seconds
	2	1.34 seconds	5.37 seconds
100 kS/s	1	11 minutes 11 seconds	44 minutes 44 seconds
	2	5 minutes 35 seconds	22 minutes 22 seconds

Onboard Signal Processing

I/Q Rate

OSP interpolation range	2, 4, 8, 12, 16, 20 24 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16) 16,384 to 32,768 (multiples of 32)
I/Q rate	(**Sample Clock rate**) ÷ (**OSP interpolation**)
Bandwith	0.4 * **I/Q rate**, per output
Data processing modes	Real (I path only) or Complex (I/Q)
OSP mode	Baseband

Prefilter Gain and Offset

Prefilter Gain and Offset Resolution	21 bits
Prefilter Gain Range	–16.0 to +16.0 (|Values| < 1 attenuate user data)
Prefilter Offset Range	–1.0 to +1.0
Prefilter Output	(User data × Prefilter gain) + Prefilter offset

Finite Impulse Response (FIR) Filtering

Table 16. FIR Parameters by Filter Type

Filter Types	Parameter	Minimum	Maximum
Flat	Passband	0.4	0.4
Raised cosine	Alpha	0.1	0.4
Root raised cosine	Alpha	0.1	0.4

Numerically Controlled Oscillator (NCO)

Maximum Frequency	0.4 * **sample rate**
Frequency Resolution	**Sample rate**/2
Tuning Speed	250 µs, typical

Digital Performance

Maximum NCO Spur	<-90 dBc
Interpolating Flat Filter Passband Ripple	<0.1 dB

Interpolating Flat Filter Out-of-Band Suppression	>80 dB

Calibration

External Calibration	The external calibration calibrates the ADC voltage reference and passband flatness. Appropriate constants are stored in nonvolatile memory.
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. Onboard channel alignment circuitry is used to calibrate the skew between channels. The self-calibration is initiated by the user through the software and takes approximately 60 seconds to complete. Appropriate constants are stored in nonvolatile memory.
Calibration Interval	Specifications valid within 1 year of external calibration
Warm-up Time	15 minutes

Power

+3.3 VDC	
Typical	1.9 A
Maximum	2.0 A
+12 VDC	
Typical	2.2 A

Maximum	2.5 A
Total power	
Typical	32.7 W
Maximum	36.6 W

Physical

Dimensions	3U, two-slot, PXI Express module 21.6 cm × 4.0 cm × 13.0 cm (8.5 in. × 1.6 in. × 5.1 in.)
Weight	476 g (17 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-25 °C to 85 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)