FS2 Frequency Synthesizer

Model AP4007A

Ultra-agile frequency synthesizer
8 kHz to 20 GHz

KEYSIGHT

Definitions

The specifications in the following pages describe the warranted performance of the instrument for 23 ±5 °C after a 30-minute warm-up period (unless otherwise stated).

Min / Max: Parameter range that is guaranteed by product design and / or production tested. Warranted performance specifications include guard-bands to account for the expected statistical performance distribution, measurement uncertainties, and changes in performance due to environmental conditions.

Typical: Expected mean values, not warranted performance.

Introduction

The FS2 Frequency Synthesizer (AP4007A) microwave signal source modules deliver instrument-grade performance, increased functionality, and efficient power consumption at a reduced size and affordable cost. The design combines low phase noise with fast switching capability, covering a wide frequency range from 8 kHz up to 20 GHz. The low spurious and harmonic content of the signal makes it ideally suitable for many demanding applications. The unit contains a high stability OCXO, providing accurate, power-calibrated, phase-lockable output signals.

The frequency resolution is 1 mHz and the power resolution is 0.01 dB power. The unit is remotely controlled with USB, LAN, or SPI control.

Due to the form-factor, the unit can also be used as a drop-in replacement of the obsolete “QuickSyn Synthesizers” from NI.

Facts, Figures, and Specifications

Signal specifications

Parameter	Min	Typical	Max	Note
Frequency range	10 MHz 8 kHz		20 GHz 20 GHz	Settable to 22.6 GHz **Option MFE**
Frequency resolution		0.001 Hz 0.001 Hz		Graphical user interface (GUI) SW setting resolution SPI interface setting resolution
Frequency switching time		500 µs 15 µs		**Option UNZ**
Phase adjustment range	0 deg		360 deg	
Phase resolution		0.1 deg		

Phase noise

CW mode, power level 15 dBm, values in dBc / Hz.

Offset frequency	10 Hz		100 Hz		1 kHz		20 kHz		100 kHz		1 MHz		10 MHz	
	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.
100 MHz	-115	-101	-139	-132	-149	-144	-156	-151	-157	-152	-157	-152	-157	-152
1 GHz	-92	-78	-121	-111	-133	-125	-140	-132	-142	-134	-143	-138	-159	-154
2 GHz	-82	-74	-116	-107	-131	-126	-140	-136	-141	-138	-137	-134	-152	-148
5 GHz	-75	-66	-107	-98	-122	-116	-131	-126	-132	-127	-131	-128	-145	-142
10 GHz	-66	-56	-102	-92	-117	-112	-126	-123	-127	-124	-126	-123	-140	-137
20 GHz	-60	-52	-96	-88	-112	-107	-121	-118	-123	-120	-121	-118	-135	-132

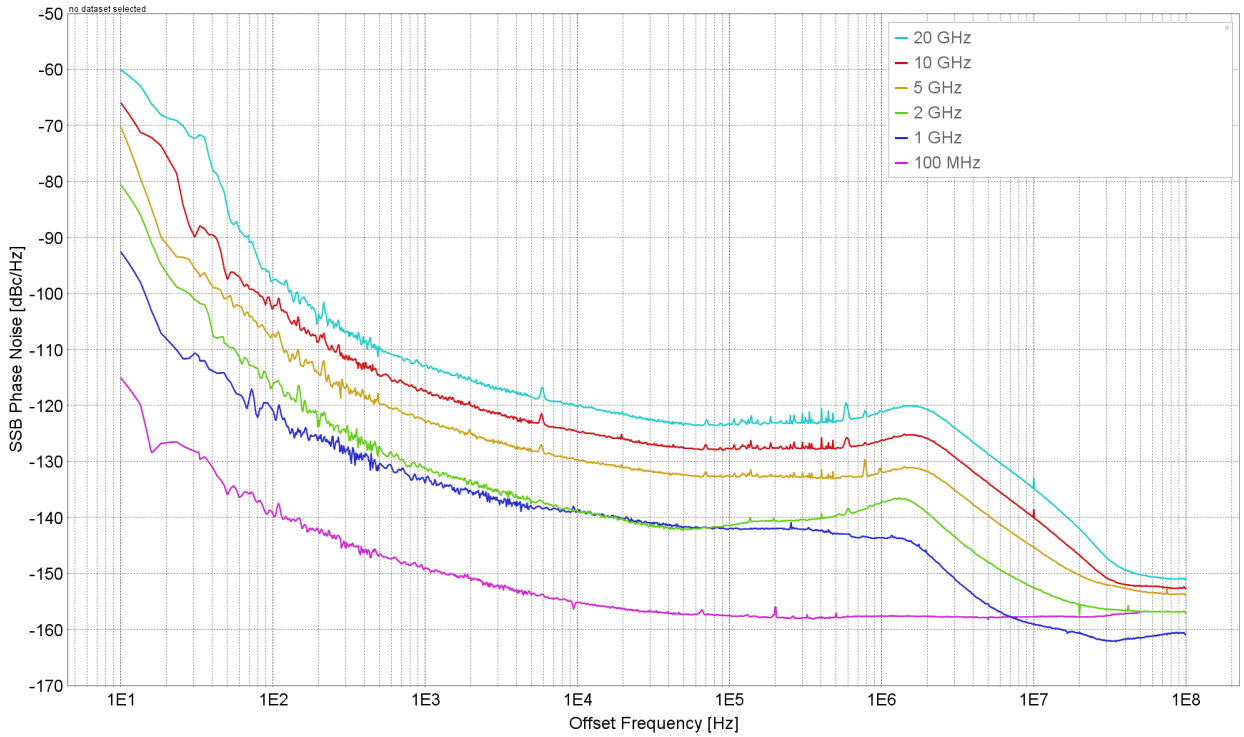


Figure 1. SSB phase noise performance

Spectral purity

Parameter	Min	Typical	Max	Note
Harmonics				At 10 dBm; See plot below
< 100 MHz		-45 dBc		
100 MHz to 2 GHz		-45 dBc	-35 dBc	
2 GHz to 20 GHz		-50 dBc	-40 dBc	
Sub-harmonics				At 10 dBm; See plot below
< 5 GHz		-75 dBc	-65 dBc	
5 GHz to 11.5 GHz		-65 dBc	-55 dBc	
11.5 GHz to 20 GHz		-75 dBc	-65 dBc	
Non-harmonic spurious				10 kHz to 0.5 GHz offset from carrier
< 1 GHz		-65 dBc		
1 GHz to 20 GHz		-70 dBc		

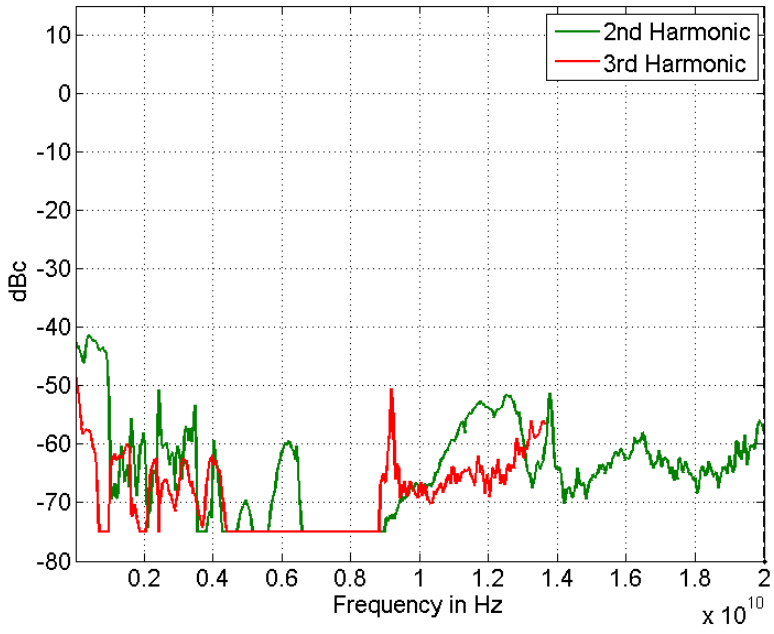


Figure 2. Harmonics (at 10 dBm output power)

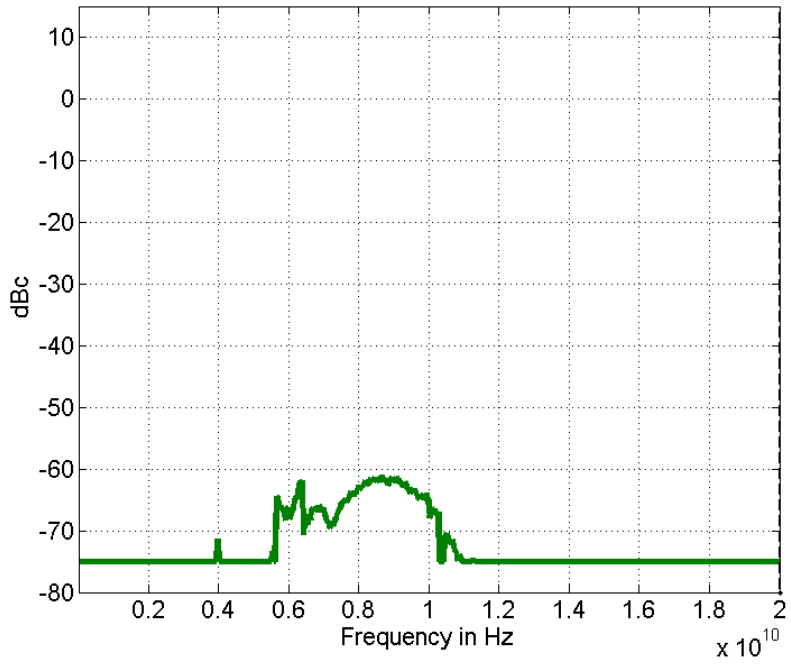


Figure 3. Subharmonics (at 10 dBm output power)

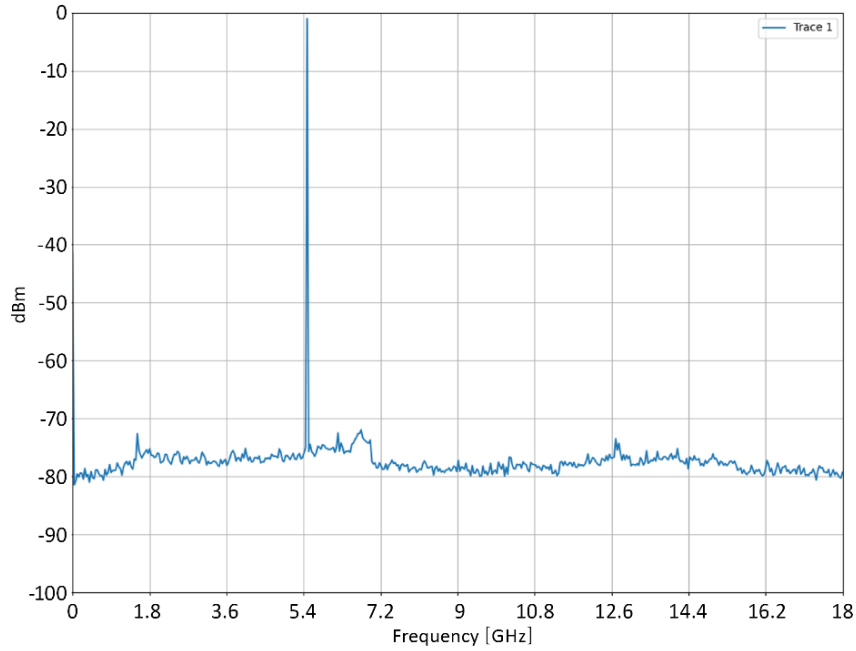


Figure 4. Wideband spectrum for 5 GHz

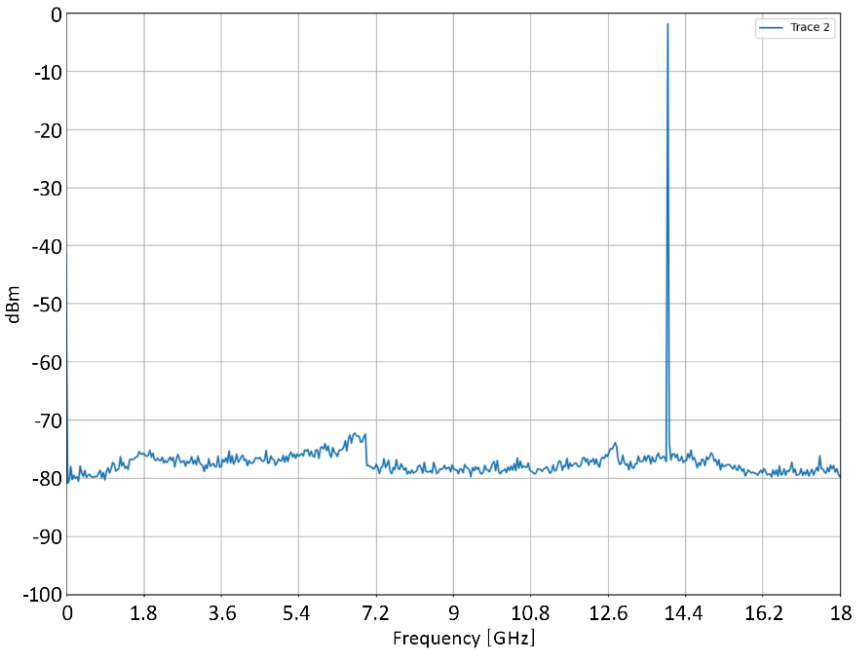


Figure 5. Wideband spectrum for 14 GHz

Level performance

Parameter	Min	Typical	Max	Note
Output power level				Settable to +30 dBm; See plot below
8 kHz to 10 MHz	-20 dBm		8 dBm	**Option MFE**
10 MHz to 20 GHz	-20 dBm		15 dBm	
Power level uncertainty		0.25 dB	1.0 dB	-20 to 15 dBm See plots below
Power resolution		0.01 dB 0.1 dB		GUI SW setting resolution SPI interface setting resolution
Power settling time		50 µs	5 µs	ALC off (open loop) ALC on (closed loop)
Output impedance		50 Ω		
VSWR		1.7		
Reverse power protection				
DC voltage			7 V	
RF power			23 dBm	

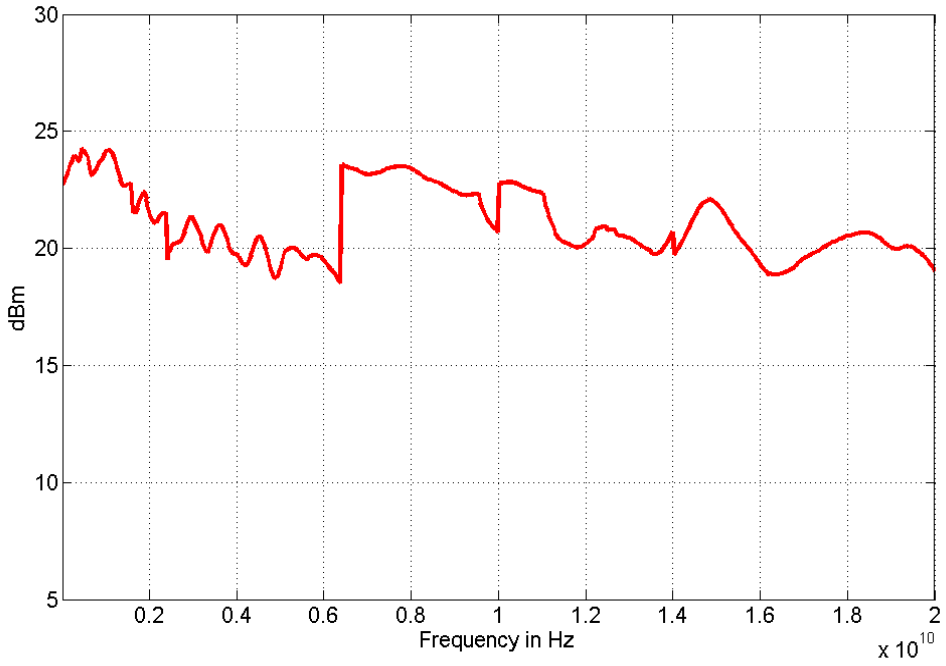


Figure 6. Maximum output power

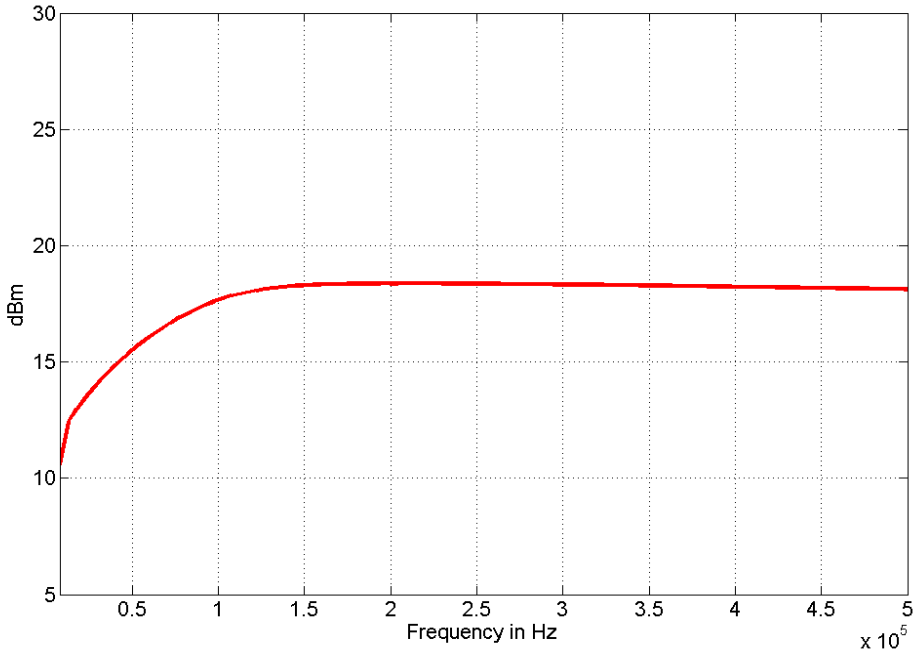


Figure 7. Maximum output power 8 kHz to 500 kHz (Option MFE)

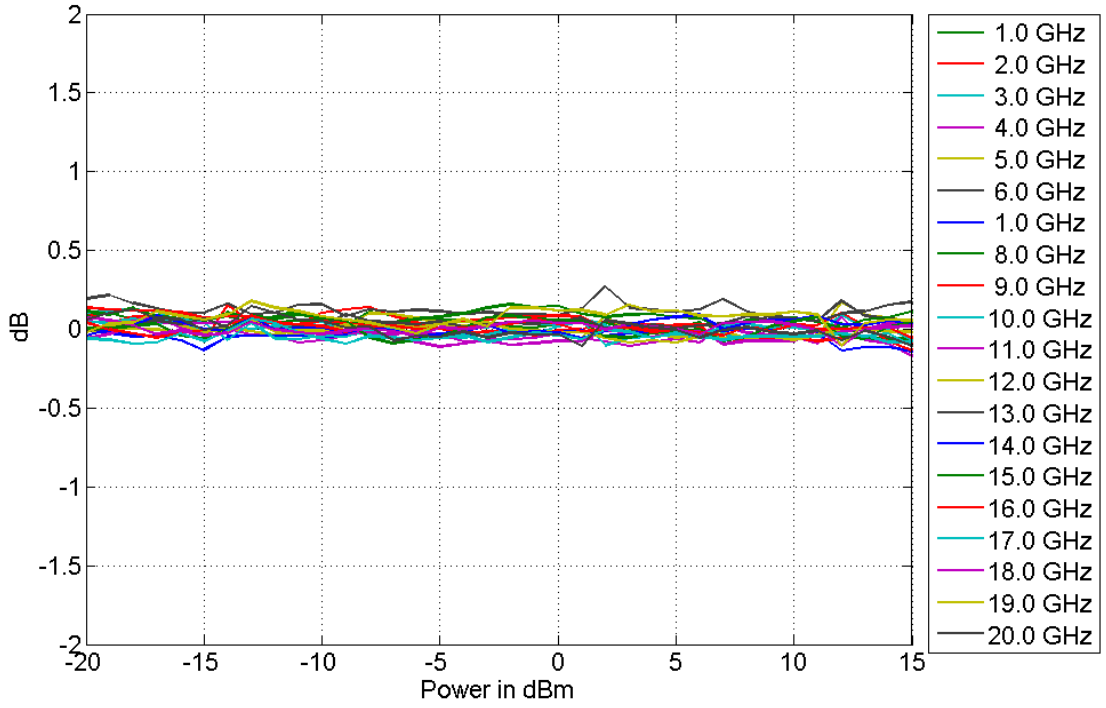


Figure 8. Power level linearity

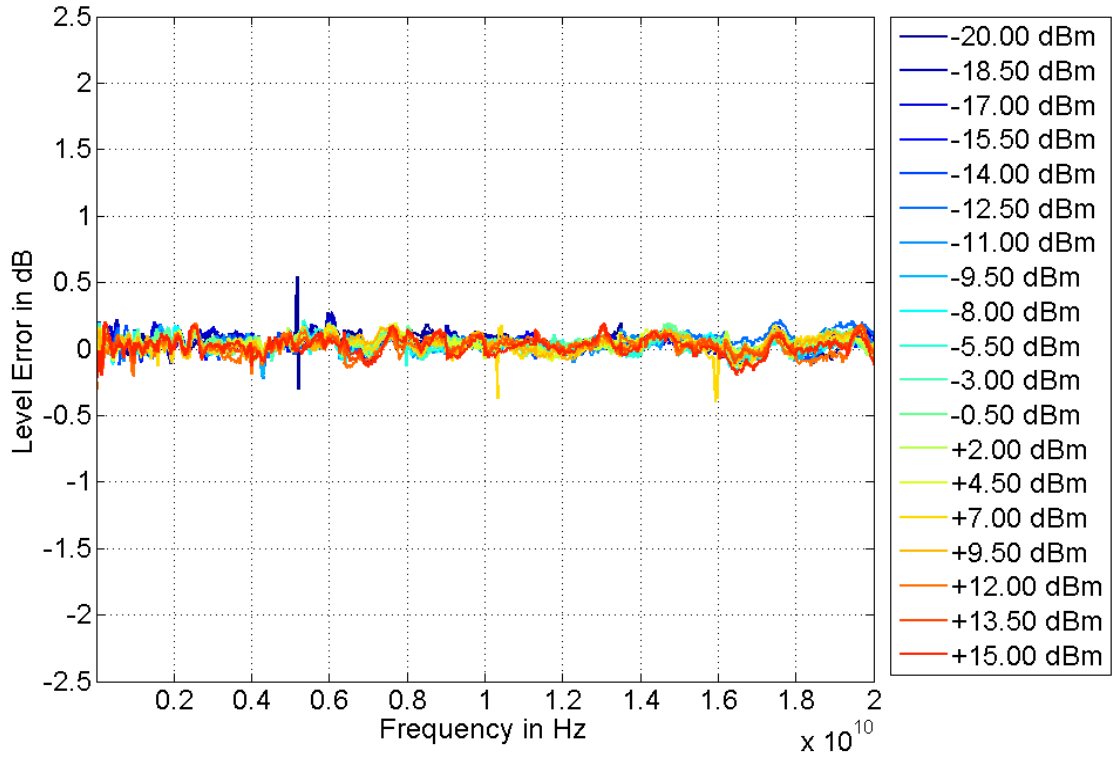


Figure 9. Frequency response

Reference frequency

Parameter	Min	Typical	Max	Note
Internal reference frequency		100 MHz		
Calibrated accuracy of int. reference		±30 ppb		Calibrated at 23 ± 3 °C
Temperature stability (0 to 40 °C)			±100 ppb	
Aging 1st year			500 ppb	
Aging per day			5 ppb	After 30 days operation
Warm-up time		5 min		
Reference frequency input	10 MHz, 100 MHz, 1 GHz 10 – 250 MHz			Fixed reference frequency Variable reference frequency
Reference input level 10 MHz 100 MHz 1 GHz 10 – 250 MHz	 -3 dBm -3 dBm -3 dBm -3 dBm		 +12 dBm +12 dBm +12 dBm +12 dBm	 Fixed reference frequency Fixed reference frequency Fixed reference frequency Variable reference frequency
Variable reference frequency resolution		100 kHz		
Lock range 10 MHz 100 MHz 1 GHz 10 – 250 MHz			 ±1.5 ppm ±100 ppm ±100 ppm ±1.5 ppm	 Fixed reference frequency Fixed reference frequency, bypass Fixed reference frequency, bypass Variable reference frequency
Reference input impedance		50 Ω		
Reference frequency output	10 MHz, 100 MHz, 1 GHz			Selectable
Output power 10 MHz 100 MHz 1 GHz	 3 dBm 3 dBm 3 dBm	 5 dBm 5 dBm 5 dBm	 7 dBm 7 dBm 7 dBm	
Reference output impedance		50 Ω		

Reference architecture
External variable reference frequencies and 10 MHz external fixed reference frequency will be internally locked to the internal 100 MHz reference with a PLL circuit. 100 MHz and 1 GHz external fixed reference frequencies are bypassing the internal reference PLL circuit and are acting directly as reference signal for the synthesizer.

Modulation capability

Parameter	Min	Typical	Max	Note
Pulse modulation				**Option PMR**
Modulation source		Internal External (PULSE)		
On / off ratio < 1 GHz 1 GHz to 6 GHz 6 GHz to 14 GHz 14 GHz to 20 GHz	 95 dB 85 dB 75 dB	 105 dB 100 dB 95 dB 90 dB		At 10 dBm; See plot below.
Pulse width compression		20 ns		
Pulse rise / fall time		9 ns		
Pulse polarity		Normal Inverse		Selectable
Pulse overshoot			10%	
External pulse latency		45 ns	60 ns	
External PULSE input threshold	0.80 V	0.88 V	0.95 V	TTL compatible
External PULSE input voltage range	-0.5 V		+5.5 V	TTL compatible 100 kΩ pull-up to +5.0 V
External PULSE input hysteresis		30 mV		
Internal pulse generator				**Option PMR**
Repetition frequency	47.6 mHz		25 MHz	=1/T
Pulse width	30 ns		21 s	Pulse width <= Pulse period
Pulse width resolution		10 ns		

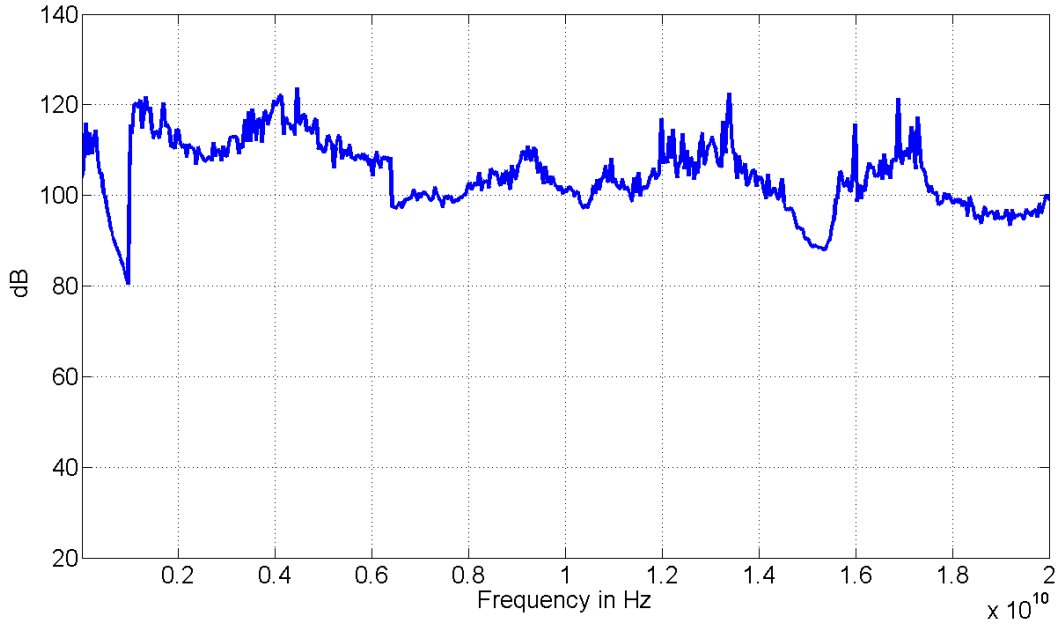


Figure 10. On / off ratio — pulse modulation (at 10 dBm output power)

Sweeping capability

Parameter	Min	Typical	Max	Note
Sweep parameters	Frequency, power, list			
Number of list points	1		50'000	
Sweep type	Linear, random			
Step time	500 µs 20 µs		21 s 21 s	**Option UNZ**
Step delay/off time	0 s		21 s	
Timing resolution		10 ns		
Timing accuracy per point		20 ns		

Generalized list sweep
Allows for individual setting of frequency, power, step-time and off-time for each point.

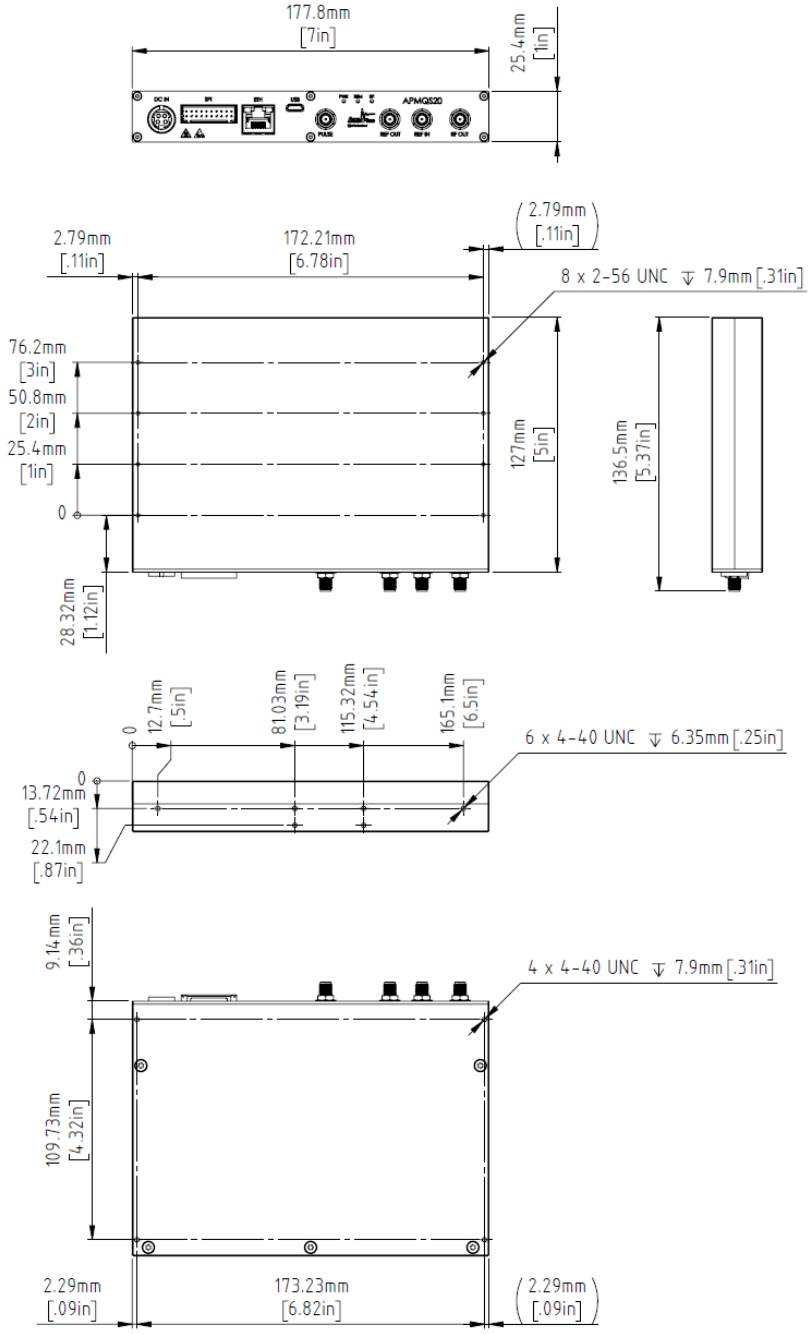
Trigger (SPI interface)

Parameter	Min	Typical	Max	Note
Trigger types		Continuous Single (point) Gated		
Trigger source		External (SPI Interface) Bus (Ethernet, USB)		
Trigger modes		Continuous free run Trigger and run		
External trigger latency		140 ns		
External trigger uncertainty		20 ns		
Trigger delay	0 s		20 s	settable
Trigger delay resolution		10 ns		
Trigger modulo	1		255	Execute only on Nth trigger event
Trigger polarity		Rising Falling		
Gated trigger polarity		Normal Inverse		

Mechanical Specifications

Dimensions and weight

Parameter	Value
Including connectors	W x L x H = 177.8 x 136.5 x 25.4 mm
Excluding connectors	W x L x H = 177.8 x 127.0 x 25.4 mm
Weight	< 1.1 kg



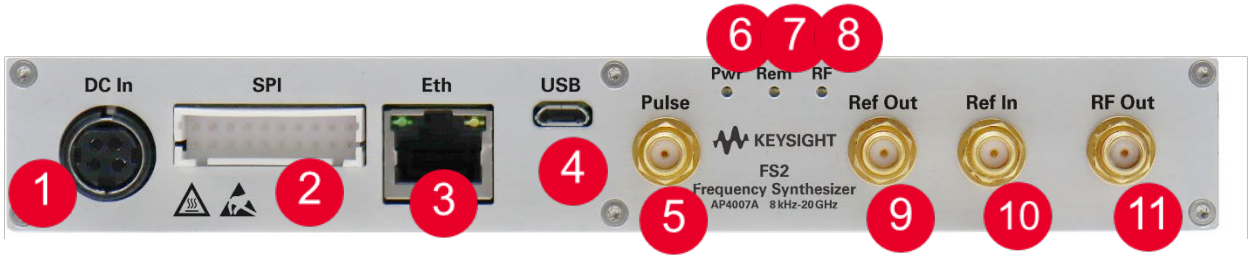
Installation instructions

The module relies on passive and/or active cooling. It is mandatory to mount the device on a heatsinking surface. Make sure the synthesizer operates under the conditions specified in this datasheet. Otherwise, the thermal protection will turn off the RF output.

Interfaces

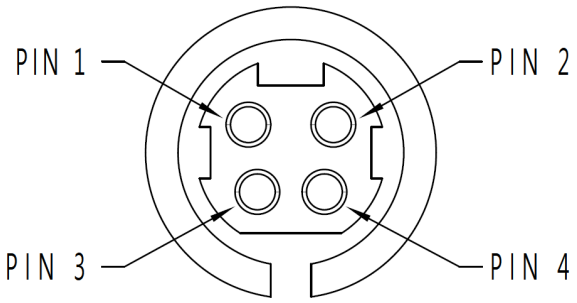
Front panel

Label	Type	Description
1. DC IN	KPJX-4S	DC input (see also chapter “Power connector assembly”). Redundant power supply input to the SPI Interface DC input (supply with higher voltage will be chosen).
2. SPI	DF1BZ-20DP-2.5DS	SPI Interface, including DC input (see also chapter “SPI interface connector assembly”)
3. ETH	RJ-45	Ethernet port
4. USB	Micro B	USB port
5. PULSE	SMA	Pulse interface, 100 kΩ pull-up to +5.0 V
6. PWR	LED	Power ON / OFF indicator
7. REM	LED	Remote connection status indicator
8. RF	LED	RF output ON / OFF indicator
9. REF OUT	SMA	Reference signal output
10. REF IN	SMA	Reference signal input
11. RF OUT	SMA	RF output



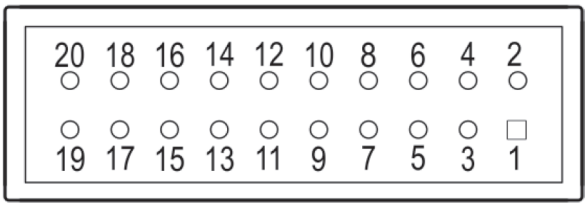
Power connector assembly

Pin	Assignment
1	GND
2	DC Supply (see also “Power requirements”)
3	GND
4	DC Supply (see also “Power requirements”)



The power connector is a 4 pin, snap and lock receptacle. Keysight recommends Kycon manufactured plugs KPPX-4P from its KPPX series.

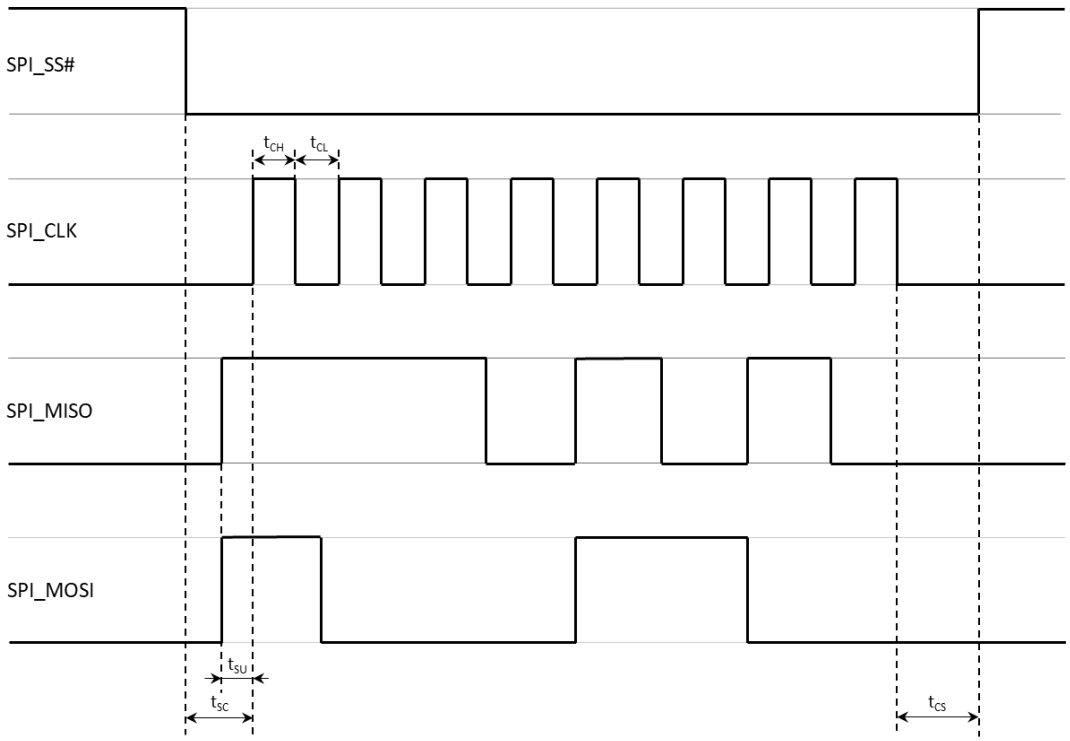
SPI interface connector assembly



Signal	Pin	Type	Description
SPI_CLK	11	Input	SPI clock. Supplied by the controlling host. The controlling host is the SPI master, the synthesizer is the SPI slave.
SPI_SS#	13	Input	SPI Slave Select. This signal is an active low input from the host to the synthesizer. It frames command communications. For each command, SPI_SS# goes low before the first bit is sent and goes high after the last bit is sent.
SPI_MISO	7	Output	Master In / Slave Out. Data line from the synthesizer to the host.
SPI_MOSI	9	Input	Master Out / Slave In. Command / Data line from the host to the synthesizer.
TRIGGER	17	Input	Edge sensitive input. The trigger signal of +3.3 V can be configured for multiple trigger modes (see also chapter “Trigger (SPI interface)”).
LOCK	15	Output	Output indicates the RF output of the synthesizer is locked on its current setting (+3.3 V locked, 0 V unlocked).
REF_LOCK	16	Output	Output indicates the synthesizer has detected an external reference signal and locked on that signal (+3.3 V locked, 0 V unlocked).
RESET#	18	Input	Internally pulled up to +3.3 V with 100 kΩ resistor. Active low signal, which has a minimum width of 1 ms, will reset the synthesizer to a default state.
DC IN	3, 4		External power supply (see also “Power requirements”). Redundant power supply input to the DC IN interface (supply with higher voltage will be chosen).
GND	8, 10, 19, 20		Ground.
DNC	1, 2, 5, 6, 12, 14		Do not connect. Reserved for factory / future use.

The SPI interface connector is a 20 pin, 2.50 mm spaced double-row header. Keysight recommends HIROSE manufactured socket DF1B-20DS-2.5RC and corresponding contacts from its DF1B series.

SPI interface timing diagram



t_{SC}	> 25 ns	SPI_SS# to be low before first clock edge
t_{CS}	> 25 ns	SPI_CLK to be low before releasing SPI_SS#
t_{SU}	> 15 ns	SPI_MISO/MOSI to be stable before rising edge of clock
t_{CH}	> 25 ns	Minimum high time of a clock pulse
t_{CL}	> 25 ns	Minimum low time of a clock pulse
f_{CLK}	≤ 12 MHz	Maximum clock frequency

Order Information

Model number	Option number	Description
AP4007A	**520**	Frequency range, 10 MHz to 20 GHz
AP4007A	**MFE**	Frequency range extension to 8 kHz
AP4007A	**UNZ**	Fast switching
AP4007A	**PMR**	Pulse modulation
AP4007A	**UK6**	Commercial calibration certificate with test data

General Characteristics

Remote programming interfaces:

1 Gbit Ethernet

USB 2.0

SPI

Control languages: SCPI Version 1999.0, native command set

Power requirements: 24 VDC; 23 W typical, 27 W maximum

Mains adapter supplied: 100 – 240 VAC, 50/60 Hz, 1.4 A max in / 24 V, 2.7 A DC out

Storage temperature range: -40 to 85 °C

Operating temperature range: 0 to 40 °C

Operating humidity range: 5 to 95% (non-condensing)

Operating altitude: up to 2,000 m

CE

Safety / EMC complies with applicable Safety and EMC regulations and directives.

Recommended calibration cycle: 24 months

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