PXIe-5451 Specifications

2023-08-09

Contents

PXIe-5451 Specifications

These specifications apply to the 128 MB, 512 MB, and 2 GBPXIe-5451.

> **Notice** To ensure the specified EMC performance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

> **Notice** To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Signals terminated with 50 Ω to ground
- Main path set to 2.5 V_{pk} differential (gain = 2.5, 5 $V_{pk\text{-}pk}$ differential)

- Direct path set to 0.5 V_{pk} differential (gain = 0.5, 1 V_{pk-pk} differential)
- Sample clock set to 400 MS/s
- Onboard Sample clock with no Reference clock
- Analog filter enabled
- 0 °C to 55 °C ambient temperature

Warranted specifications are valid under the following conditions unless otherwise noted.

- 15 minutes warm-up time at ambient temperature
- Calibration cycle maintained
- Chassis fan speed set to High
- NI-FGEN instrument driver used
- NI-FGEN instrument driver self-calibration performed after instrument is stable

Typical specifications are valid under the following conditions unless otherwise noted:

- Over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production

Analog Outputs

CH 0+/–, CH 1+/– (Analog Outputs, Front Panel Connectors)

Number of channels	2
Output type	Single Ended, Differential
Output paths	Main path, Direct path

DAC resolution	16

Amplitude and Offset

Amplitude resolution	4 digits, <0.0025% (0.0002 dB of amplitude range)
Offset resolution	4 digits, < 0.002% of offset range

Full-Scale Amplitude Range

Table 1. Full-Scale Amplitude Range

Flatness Correction State	Load	Amplitude					
		Single-Ended Main Path		Differential Main Path		Differential Direct Path	
		Min. (V_{PPSE})	Max. (V_{PPSE})	Min. (V_{PPD})	Max. (V_{PPD})	Min. (V_{PPD})	Max. (V_{PPD})
Disabled	50 Ω	0.00176	2.50	0.00352	5.00	0.708	1.00
	1 kΩ	0.00336	4.76	0.00671	9.52	1.35	1.9
	Open	0.00352	5.00	0.00705	10.00	1.42	2.00
Enabled	50 Ω	0.00124	1.75	0.00247	3.50	0.567	0.8
	1 kΩ	0.00235	3.33	0.00470	6.66	1.08	1.52
	Open	0.00247	3.50	0.00493	7.00	1.14	1.6

Analog Offset Range

Table 2. Analog Offset Range, Per Terminal

Load	Amplitude ,	
	Main Path	Direct Path
50 Ω	±1.00	—
1 kΩ	±1.905	—
Open	±2.00	—

Accuracy

Channel-to-channel timing alignment accuracy	
Main path	50 ps; 40 ps, typical
Direct path	35 ps; 25 ps, typical

DC Accuracy

Table 3. Absolute Gain Error

Temperature Range	Single-Ended Main Path	Differential Main Path	Differential Direct Path
Within ±5 °C of Self-Cal temperature	±(0.4% of single-ended output range + 0.5 mV) ±(0.3% of single-ended output range + 0.3 mV), typical	±(0.6% of differential output range + 1 mV) ±(0.43% × differential output range + 500 µV), typical	±0.2% of differential output range
Outside ± 5 °C of Self-Cal temperature	-0.05%/°C -0.035%/°C, typical	-0.05%/°C -0.035%/°C, typical	+0.030%/°C +0.015%/°C, typical

Absolute single-ended Main path offset error (0 °C to 55 °C)	±(0.15% of offset + 0.04% of single-ended output range + 1.25 mV) ±(0.08% of offset + 0.025% of single-ended output range + 0.75 mV), typical
Absolute differential offset	
Differential Main path	±(0.3% of differential offset + 0.01% of differential output range + 2 mV) ±(0.16% of differential offset + 0.01% of differential output range + 1 mV), typical

Differential Direct path (0 °C to 55 °C)	±1 mV
Absolute common-mode offset	
Differential Main path	±(0.3% of common-mode offset + 2 mV) ±(0.16% of common-mode offset + 1 mV), typical
Differential Direct path (0 °C to 55 °C)	±350 µV

Table 4. Channel-to-Channel Relative Gain Error

Temperature Range	Differential Main Path	Differential Direct Path
Within ±5 °C of Self-Cal temperature	±(0.66% of differential output range + 1.75 mV)	±0.08% of differential output range
Outside ±5 °C of Self-Cal temperature	-0.02%/°C -0.01%/°C, typical	+0.010%/°C +0.005%/°C, typical

AC Amplitude Accuracy

Absolute AC amplitude accuracy	
Single-ended Main path	±(0.8% of single-ended output range + 1 mV_{RMS}) ±(0.4% of single-ended output range + 750 μV_{RMS}), typical
Differential Main path	±(0.8% of differential output range + 1.5 mV_{RMS}) ±(0.4% of differential output range + 1.5 μV_{RMS}), typical
Differential Direct path	±0.5% of differential output range

Channel-to-channel, relative AC amplitude accuracy	±0.2% of differential output range ±0.07% of differential output range, typical

Output Characteristics

DC output resistance	
Main path	50 Ω nominal, per connector
Direct path	50 Ω nominal, per connector
Return loss (Nominal)	
Single-ended and differential Main path	
Up to 20 MHz	30 dB
Up to 60 MHz	27 dB
Up to 135 MHz	12 dB
Single-ended Direct path	
5 MHz to 60 MHz	26 dB
60 MHz to 145 MHz	15 dB
Differential Direct path	
Up to 20 MHz	35 dB
Up to 60 MHz	22 dB
Up to 145 MHz	12 dB

Load impedance compensation	Output amplitude is compensated for user-specified load impedance to ground. Performed in software.
Output coupling	DC
Output enable	Software-selectable. When disabled, output is terminated with a 50 Ω, 1 W resistor.
Maximum output overload	
Main path	±12 V_{pk} from a 50 Ω source
Direct path	±8 V_{pk} from a 50 Ω source
Waveform summing	The output terminals support waveform summing, which means the outputs of multiple PXIe-5451 signal generators can be connected together.

Frequency Response

Table 5. Analog Bandwidth, Typical

Path	Baseband	Complex Baseband
Main Path, Filter Disabled	180 MHz for each I and Q output	360 MHz when used with external I/Q modulator
Main Path, Filter Enabled	135 MHz for each I and Q output	270 MHz when used with external I/Q modulator
Direct Path	145 MHz for each I and Q output	290 MHz when used with external I/Q modulator

Analog filter	
Main path	7-pole elliptic filter for image suppression
Direct path	4-pole filter for image suppression

Table 6. Passband Flatness

Frequency Range	Channel-to-Channel Passband Flatness Matching Enabled	Single-Ended and Differential Main Path, Filter Enabled		Direct Path	
		Flatness Correction Disabled	Flatness Correction Enabled	Flatness Correction Disabled	Flatness Correction Enabled
0 MHz to 60 MHz	No	0.8 dB, typical	±0.30 dB ±0.20 dB, typical	0.5 dB, typical	±0.24 dB ±0.13 dB, typical
	Yes	±0.12 dB, typical	±0.12 dB typical	0.05 dB, typical	0.03 dB, typical
60 MHz to 135 MHz	No	3 dB, typical	±0.50 dB ±0.30 dB, typical	1.9 dB, typical	±0.34 dB ±0.19 dB, typical
	Yes	±0.20 dB, typical	±0.14 dB typical	0.18 dB, typical	0.04 dB, typical

Figure 1. Main Path Filter Enabled Amplitude Response with Flatness Correction Enabled and Disabled, 400 MS/s, Gain = 2.5, Differential, Referenced to 50 kHz, Representative Unit

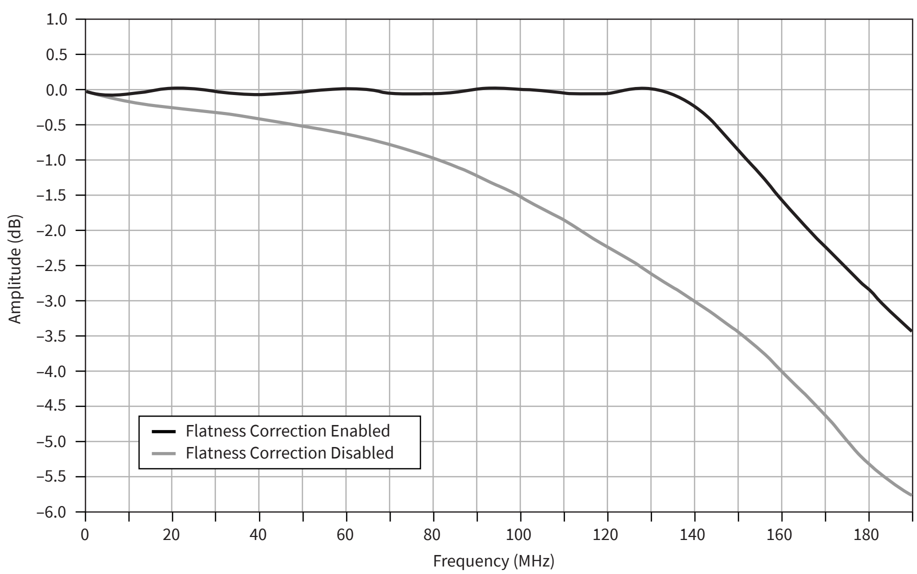


Figure 2. Direct Path Amplitude Response with Flatness Correction Enabled and Disabled,400 MS/s, Differential, Referenced to 50 kHz, Representative Unit

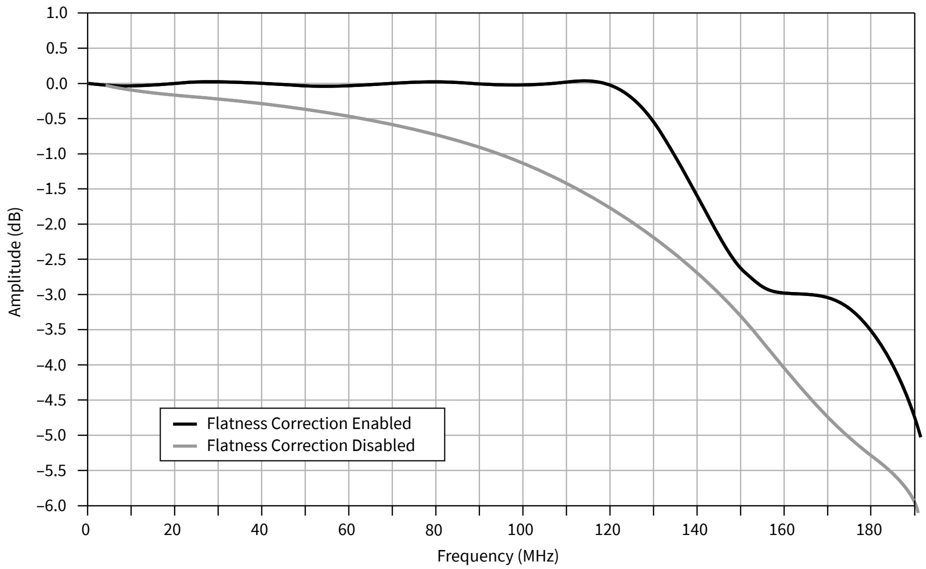


Figure 3. Main and Direct Path Amplitude Response with Flatness Correction Enabled, 400 MS/s, Differential, Referenced to 50 kHz, Representative Unit

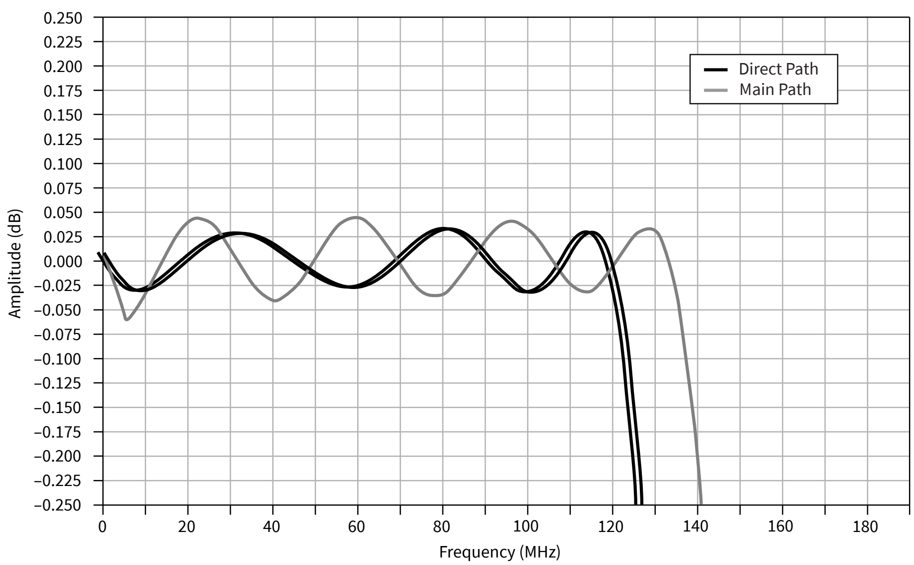


Figure 4. Main Path Characteristic Frequency Response of Image Suppression Filter, Representative Unit

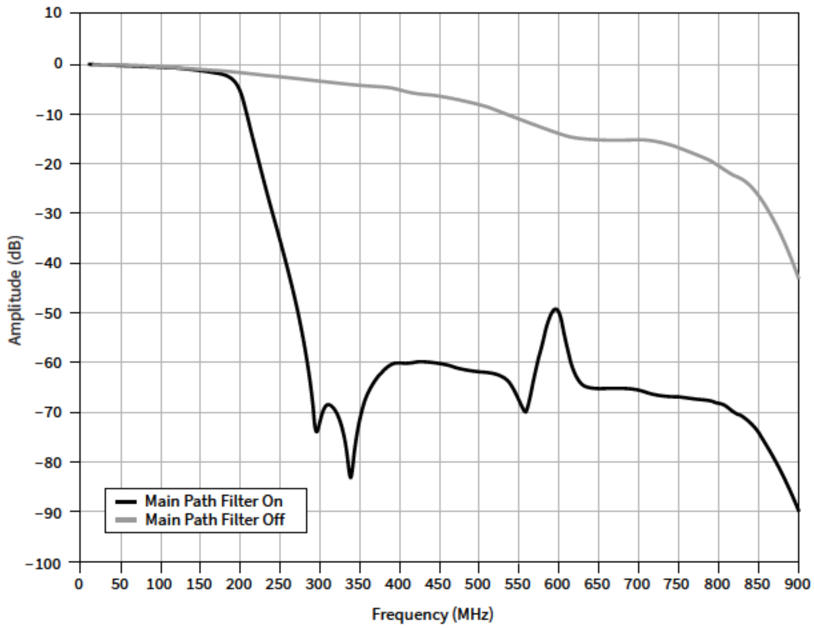
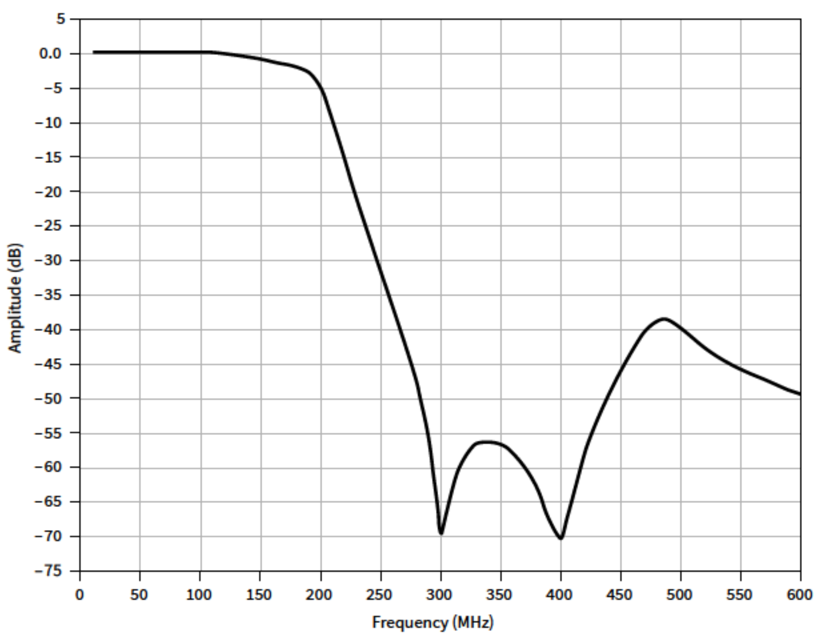


Figure 5. Direct Path Characteristic Frequency Response of Image Suppression Filter, Representative Unit



Note Sinc response due to DAC sampling is not included in the previous two figures.

Spectral Characteristics

Table 7. Nominal Spurious Free Dynamic Range (SFDR) at 1 MHz

	Frequency Range	Single-Ended Main Path			Differential Main Path			Differential Direct Path
		Gain = 0.25 0.5 V_{PPSE}	Gain = 0.625 1.25 V_{PPSE}	Gain = 1.25 2.5 V_{PPSE}	Gain = 0.5 1 V_{PPD}	Gain = 1.25 2.5 V_{PPD}	Gain = 2.5 5 V_{PPD}	Gain = 0.5 1 V_{PPD}
SFDR With Harmonics (dB)	DC to 7 MHz	82			85			88
	DC to 200 MHz	75			75			75
SFDR Without Harmonics (dB)	DC to 7 MHz	82	88	95	98			98
	DC to 200 MHz	82	83	84	84			84

Table 13. Typical Spurious Free Dynamic Range (SFDR) from DC to 200 MHz

	Frequency	Single-Ended Main Path			Differential Main Path			Differential Direct Path
		Gain = 0.25 0.5 V_{PPSE}	Gain = 0.625 1.25 V_{PPSE}	Gain = 1.25 2.5 V_{PPSE}	Gain = 0.5 1 V_{PPD}	Gain = 1.25 2.5 V_{PPD}	Gain = 2.5 5 V_{PPD}	Gain = 0.5 1 V_{PPD}
SFDR With Harmonics (dB)	10 MHz	73 (75)	73 (75)	73 (75)	73 (75)	73 (75)	73 (73)	73 (75)
	60 MHz	65	61	56	69	67	64	70 (72)
	100 MHz	53	52	49	55	54	53	60
	120 MHz	62	62	62	62	62	62	62
	160 MHz	—						62

	Frequency	Single-Ended Main Path			Differential Main Path			Differential Direct Path
		Gain = 0.25 0.5 V_{PPSE}	Gain = 0.625 1.25 V_{PPSE}	Gain = 1.25 2.5 V_{PPSE}	Gain = 0.5 1 V_{PPD}	Gain = 1.25 2.5 V_{PPD}	Gain = 2.5 5 V_{PPD}	Gain = 0.5 1 V_{PPD}
SFDR Without Harmonics (dB)	10 MHz	74 (76)						74 (76)
	60 MHz	72 (74)						72 (74)
	100 MHz	66						64
	120 MHz	62						62
	160 MHz	—						62

Table 9. Out-of-Band Performance (Nominal)

In-Band Tone Frequency (MHz)	Out-of-Band Spur Level (dBm)	
	Main Path, Filter Enabled	Direct Path
0 MHz to 20 MHz	<–65 dBm	<–80 dBm
20 MHz to 50 MHz	<–45 dBm	<–65 dBm

Table 10. Channel-to-Channel Crosstalk (Nominal)

Aggressor Output Amplitude	Main Path (0 MHz to 200 MHz)	Direct Path	
		0 MHz to 150 MHz	0 MHz to 200 MHz
2.5	–90 dBc	<90 dBc	<80 dBc
1.25	–85 dBc		
0.5	–80 dBc		
0.15	–70 dBc		

Table 11. Typical Total Harmonic Distortion (THD)

Output Amplitude	Frequency (MHz)	THD (dBc)		
		Main Path		Direct Path
		Single-Ended	Differential	
2.5 V_{PPSE}, 5 V_{PPD}	10	–71	–71	—
	20	–66	–69	

Output Amplitude	Frequency (MHz)	THD (dBc)		
		Main Path		Direct Path
		Single-Ended	Differential	
	40	–59	–64	
	60	–55	–61	
	80	–51	–55	
	120	–50	–51	
	140	–50	–52	
	160	–50	–53	
1.25 V_{PPSE}, 2.5 V_{PPD}	10	–78	–75	
	20	–72	–73	
	40	–63	–69	
	60	–60	–65	
	80	–56	–59	
	120	–56	–59	
	140	–56	–59	
	160	–55	–59	
0.5 V_{PPSE}, 1 V_{PPD}	10	–80	–79	–75
	20	–74	–75	–70
	40	–68	–69	–68
	60	–64	–69	—
	80	–62	–65	–68
	100	—	—	–68
	120	–65	–70	–78
	140	–64	–69	—
	160	–61	–66	–83

Figure 6. Direct Path, Total Harmonic Distortion, Typical

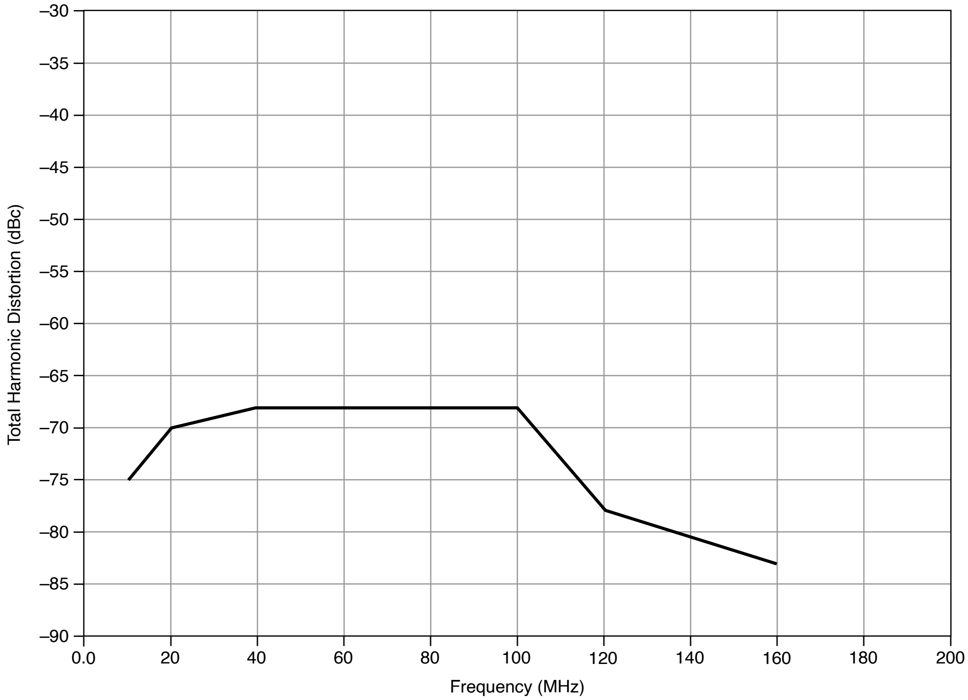


Figure 7. Single-Ended Main Path, Total Harmonic Distortion, Typical

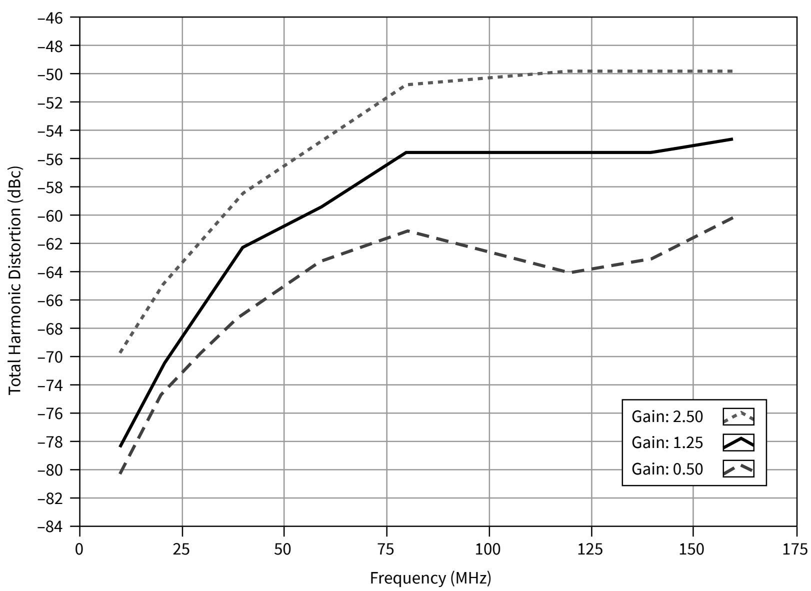


Figure 8. Differential Main Path, Total Harmonic Distortion, Typical

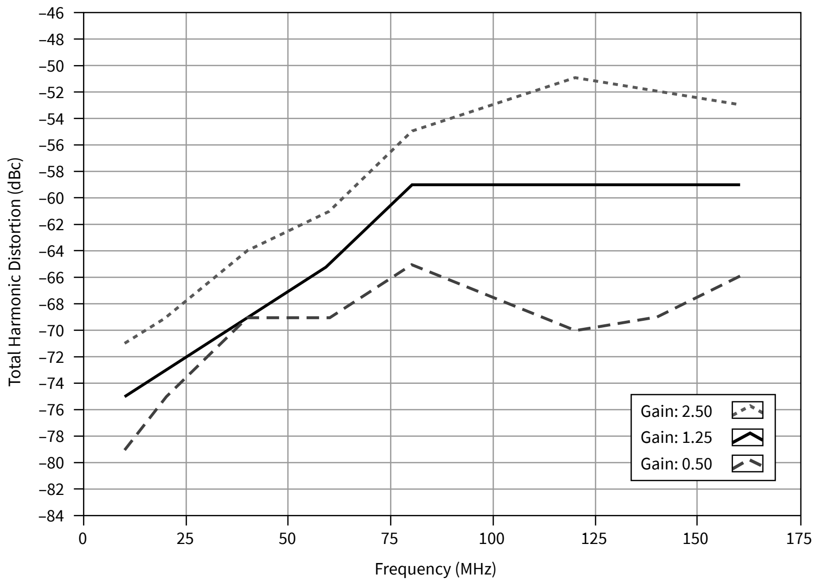


Table 12. Typical Intermodulation Distortion (IMD_3)

Output Amplitude	Frequency (MHz)	IMD (dBc)	
		Single-Ended and Differential Main Path	Direct Path
2.5 V_{PPSE}, 5 V_{PPD}	10	–87	—
	20	–82	
	40	–71	
	60	–63	
	80	–57	
	120	–51	
	160	–48	
1.25 V_{PPSE}, 2.5 V_{PPD}	10	–92	
	20	–87	
	40	–79	
	60	–72	
	80	–66	
	120	–61	
	160	–57	
0.5 V_{PPSE}, 1 V_{PPD}	10	–87	–84

Output Amplitude	Frequency (MHz)	IMD (dBc)	
		Single-Ended and Differential Main Path	Direct Path
	20	−85	−81
	40	−82	−75
	60	−79	—
	80	−75	−71
	100	—	−68
	120	−79	−68
	160	−75	−66
0.1 V_{PPSE}, 0.2 V_{PPD}	10	−89	—
	20	−83	
	40	−78	
	60	−73	
	80	−69	
	120	−66	
	160	−65	

Figure 9. Single-Ended and Differential Main Path, Intermodulation Distortion, 200 kHz Separation, Typical

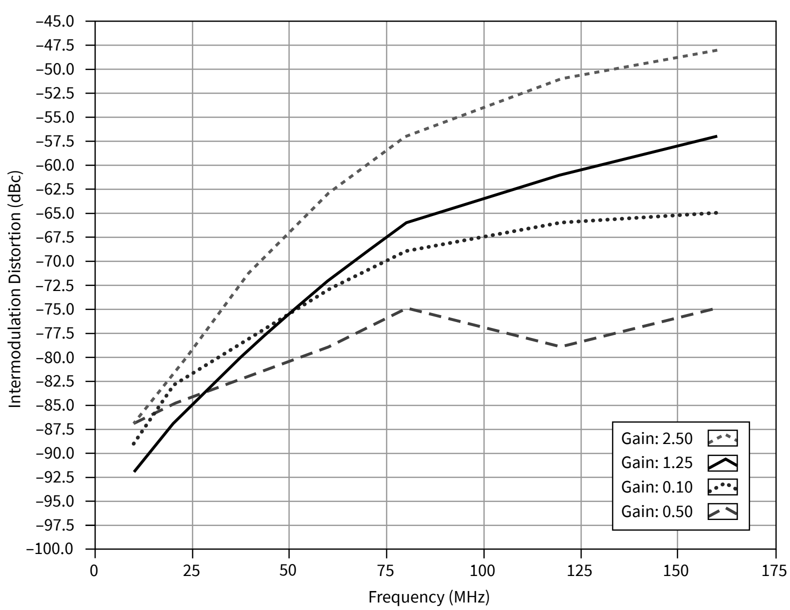


Figure 10. Direct Path, Intermodulation Distortion, 200 kHz Separation, Typical

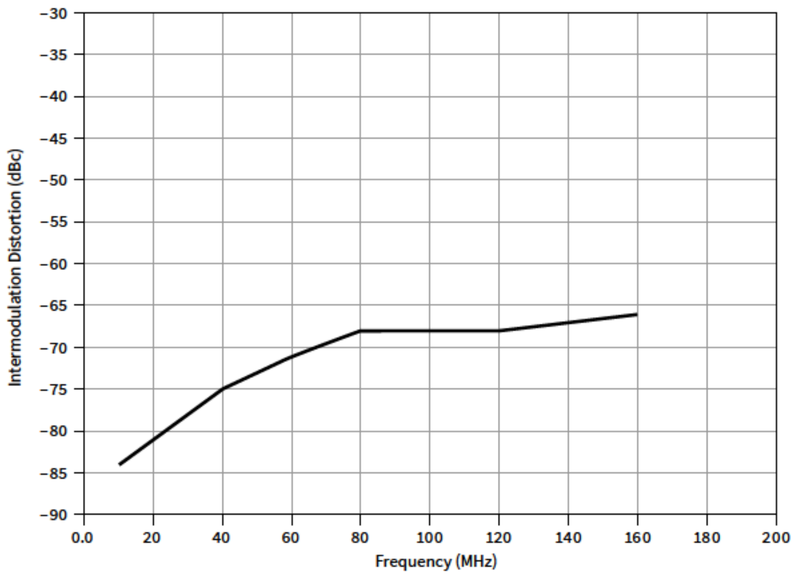


Table 13. Average Noise Density

Path	Output Amplitude		Average Noise Density		
	V_{PPSE}	dBm	Object Missing This object is not available in the repository.	dBm/Hz	dBFS/Hz
Single-Ended Main Path	2.5	12	12.57	−145	−157
	0.5	−2	9.99	−147	−145
	0.06	−20.4	9.99	−147	−126.6
Differential Main Path	5	18	17.76	−142	−160
	1	4	14.11	−144	−148
	0.12	−14.4	14.11	−144	−129.6
Differential Direct Path	1	4.0	2.24	−160	−164

Figure 11. Single-Ended Main Path 10.000 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit

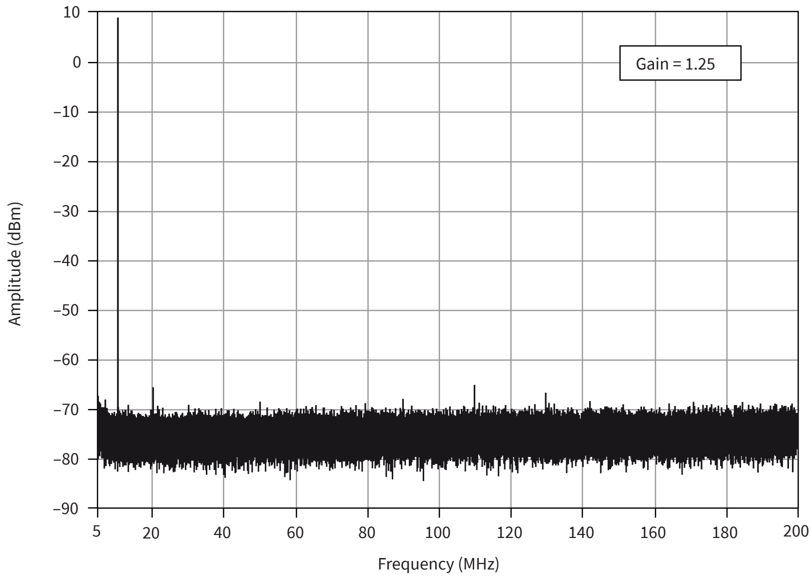


Figure 12. Single-Ended Main Path 10.100 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit

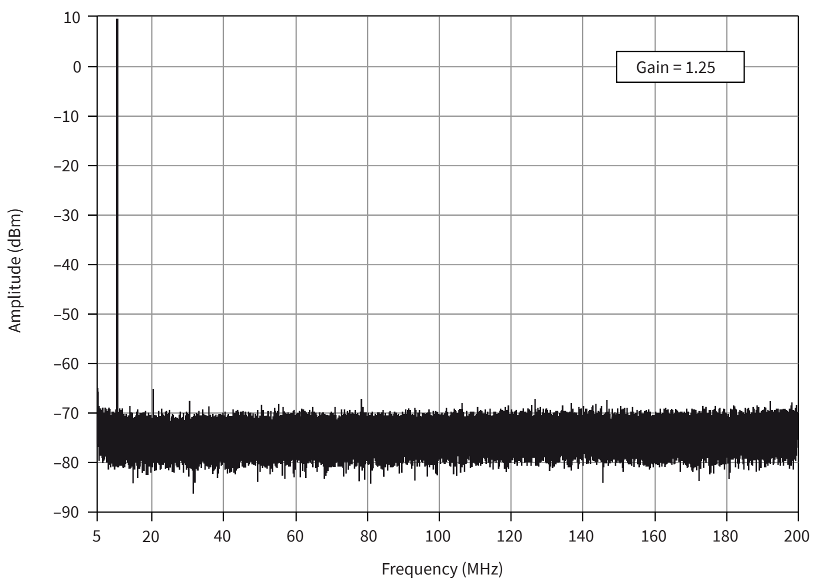


Figure 13. Single-Ended Main Path 110.100 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit

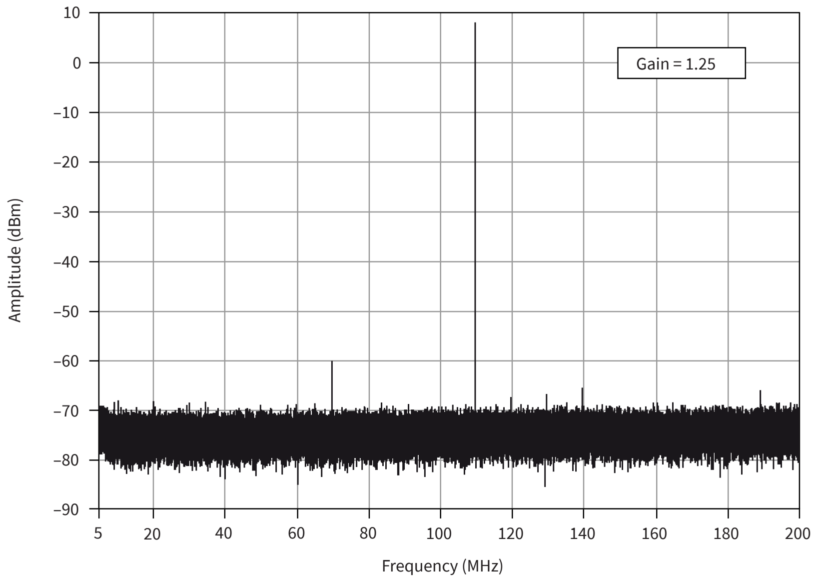


Figure 14. Differential Main Path 10.000 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, measured through a balun, Representative Unit

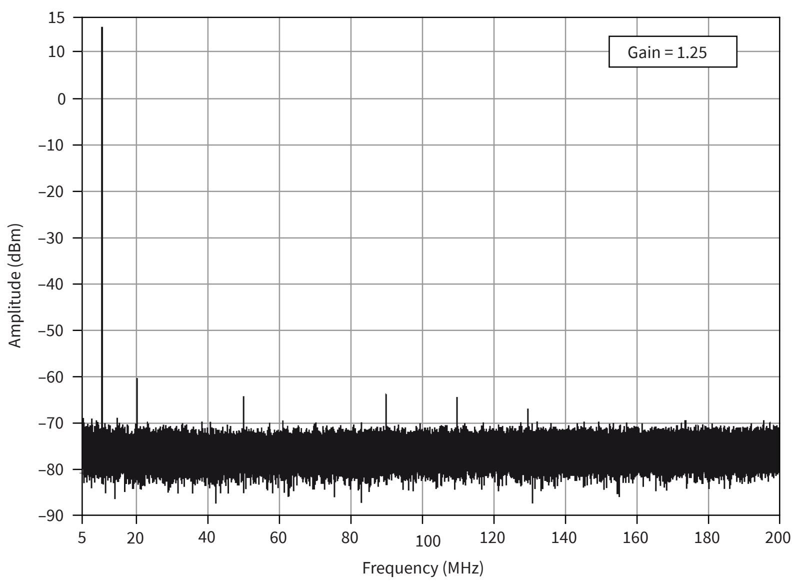


Figure 15. Single-Ended Main Path Intermodulation Distortion, 1 MHz Separation, 20 MHz Tone, 400 MS/s, – 7 dBFS, Representative Unit

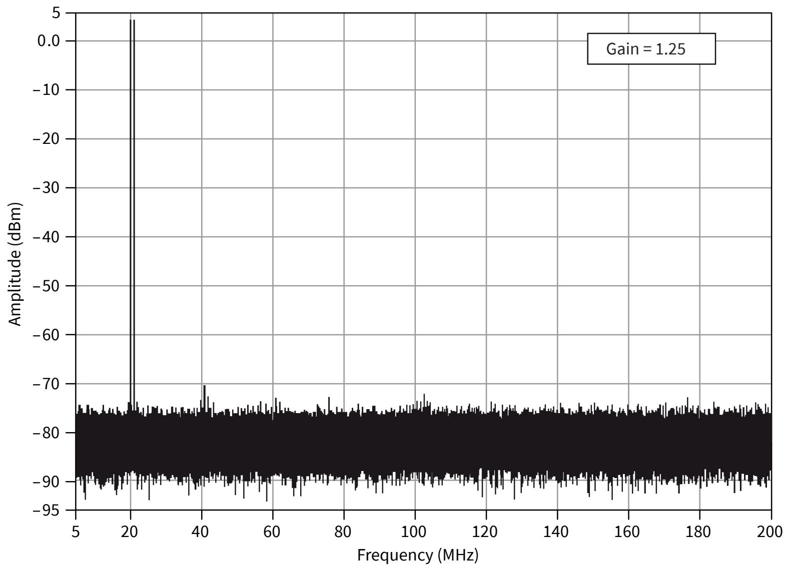


Figure 16. Direct Path Intermodulation Distortion, 1 MHz Separation, 20 MHz Tone, 400 MS/s, – 7 dBFS, Representative Unit

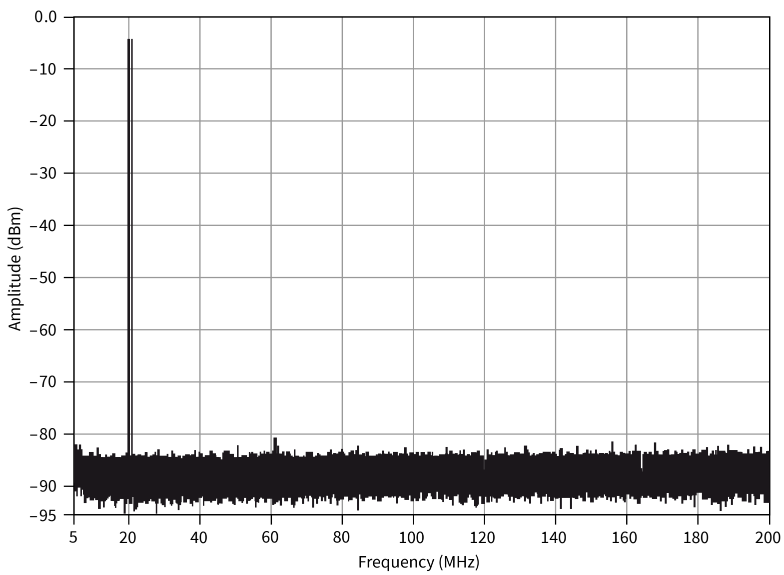


Figure 17. Direct Path 10.000 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit

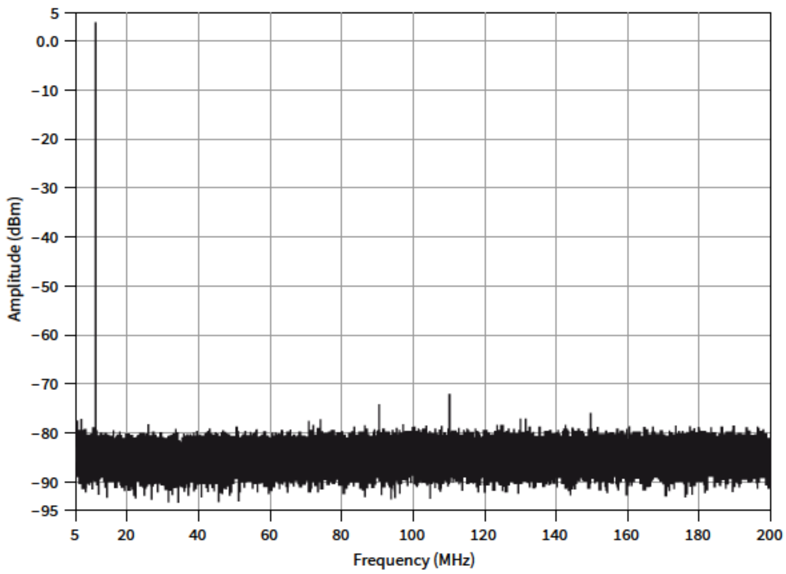
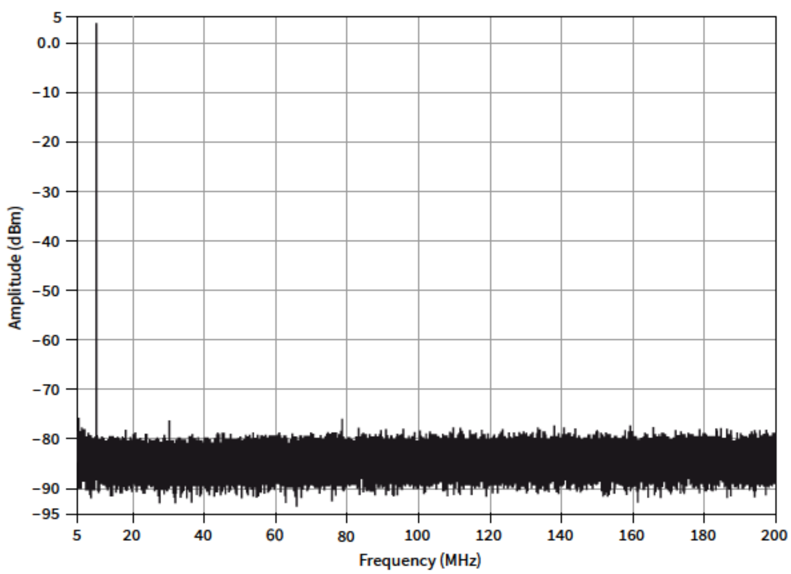


Figure 18. Direct Path 10.100 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit



Note The noise floor on all spectral graphs is limited by the measurement device.

Output Phase Noise and Jitter

Table 14. Typical Output Phase Noise and Jitter

Sample Clock Source	Output Freq. (MHz)	System Phase Noise Density (dBc/Hz)					System Output Integrated Jitter (fs)
		100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	
Internal, High Resolution Clock, 400 MS/s	10	<–121	<–137	<–146	<–152	<–153	<350
	100	<–101	<–119	<–126	<–136	<–141	<350
CLK IN External 10 MHz Reference Clock,400 MS/s	10	<–122	<–135	<–146	<–152	<–153	<350
	100	<–105	<–115	<–126	<–136	<–141	<350

Figure 19. Phase Noise on a Representative Module, 100 MHz Sine Wave, 400 MS/s Internal Clock Sample Rate, Chassis Fans Low, Shown With and Without a Reference Clock

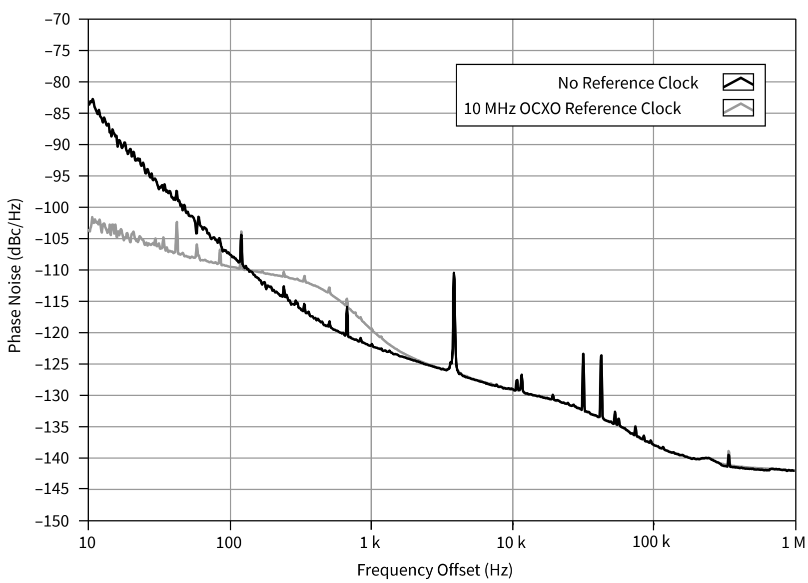
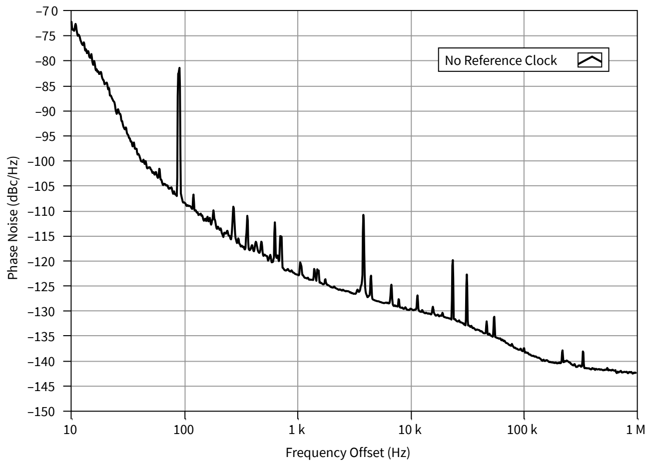


Figure 20. Phase Noise on a Representative Module, 100 MHz Sine Wave, 400 MS/s Internal Clock Sample Rate, Chassis Fans High, No Reference Clock



Suggested Maximum Frequencies for Common Functions

Table 15. Suggested Maximum Frequencies

Function	Main Path	Direct Path
Sine	135 MHz	145 MHz
Square	150 MHz	33 MHz (<133 V/µs slew rate)
Ramp	20 MHz	1 MHz (< 50 V/µs slew rate)
Triangle	20 MHz (5 MHz)	8 MHz

Pulse Response

Table 16. Typical Rise/Fall Time (10% to 90%)

Flatness Correction	Main Path		Direct Path
	Filter Disabled	Filter Enabled	
Flatness Correction Disabled	1.5 ns	3 ns	3 ns
Flatness Correction Enabled	—	3 ns	2.5 ns

Table 17. Typical Aberration

Flatness Correction	Main Path		Direct Path
	Filter Disabled	Filter Enabled	
Flatness Correction Disabled	3%	18%	18% (7%)
Flatness Correction Enabled	—	25%	22%

Clocking

Onboard Sample Clock

Sample clock rate range	12.2 kS/s to 400 MS/s
Sample clock rate frequency resolution	<5.7 μHz
Sample clock delay	0 ns to 2 ns, independent per channel
Sample clock delay resolution	10 ps nominal
Sample clock timebase phase adjust	±1 Sample clock timebase period

External Sample Clock

External Sample clock source	CLK IN front panel connector, with multiplication and division
External Sample clock rate	10 MS/s, 20 MS/s to 400 MS/s
Sample Clock rate range	12.2 kS/s to 400 MS/s

Multiplication/Division factor range	Varies depending on the external Sample clock rate
External Sample clock delay	0 ns to 2 ns, independent per channel
External Sample clock delay resolution	10 ps, nominal
External Sample clock timebase phase adjust	±1 Sample clock timebase period

External Sample Clock Timebase

External Sample clock timebase sources	CLK IN front panel connector, with division
External Sample clock timebase rate range	200 MS/s to 400 MS/s
Divide factor range	1, 2 to 32768 in steps of 2
Sample Clock delay	0 ns to 2 ns, independent per channel
Sample Clock delay resolution	10 ps nominal

Reference Clock

Reference clock sources	None (internal reference), PXI_CLK10 (backplane), or CLK IN (front panel connector)
Reference clock frequency	
In increments of 1 MHz	1 MHz to 100 MHz
In increments of 2 MHz	100 MHz to 200 MHz
In increments of 4 MHz	200 MHz to 400 MHz

Internal reference clock frequency accuracy	± 0.01%

Exporting Clocks

Table 18. Exported Clock Rates

Clock	Destination	Rates
Reference Clock	CLK OUT	1 MHz to 400 MHz
	PFI<0..1>	1 MHz to 200 MHz
Sample Clock	CLK OUT	100 kHz to 400 MHz
	PFI<0..1>	0 MHz to 200 MHz
Sample Clock Timebase	CLK OUT	100 kHz to 400 MHz
	PFI<0..1>	0 MHz to 200 MHz

Terminals

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Direction	Input
Destinations	Reference clock, Sample clock, or Sample clock timebase
Frequency range	1 MHz to 400 MHz
Input impedance	50 Ω , nominal
Input voltage range	
50% duty cycle input	500 mVpk-pk to 5 Vpk-pk into 50 Ω (–2 dBm to +18 dBm)

45% to 55% duty cycle input	550 mVpk-pk to 4.5 Vpk-pk into 50 Ω (–1.2 dBm to +17 dBm)
Input protection range	
50% duty cycle input	6 V_{pk-pk} into 50 Ω (19.5 dBm)
45% to 55% duty cycle input	5.4 V_{pk-pk} into 50 Ω (18.5 dBm)
Duty cycle requirements	45% to 55%
Input coupling	AC
Voltage standing wave ratio (VSWR)	1.3:1 up to 2 GHz, nominal

CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)

Direction	Output
Sources	Sample clock, divided by integer K (1≤ K ≤ 3, minimum), Reference clock, or Sample clock timebase, divided by integer M (1 ≤ M ≤ 1048576)
Frequency Range	100 kHz to 400 MHz
Output Voltage	≥0.7 V_{pk-pk} into 50 Ω typical
Maximum Output Overload	3.3 V_{pk-pk} from a 50 Ω source
Output Coupling	AC

VSWR	1.3:1 up to 2 GHz nominal

PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Direction	Bidirectional
Frequency Range	DC to 200 MHz
As an Input (Trigger)	
Destinations	Start trigger, Script trigger
Input Range	0 V to 5 V
Input Protection Range	-2 V to +6.5 V
Input voltage	
V_{IH}	1.8 V
V_{IL}	1.5 V
Input Impedance	10 kΩ , nominal
As an Output (Event)	
Sources	Sample clock divided by integer K ($2 \leq K \leq 3$, minimum), Sample clock timebase divided by integer M ($2 \leq M \leq 1048576$), Reference clock, Marker event, Data marker event, Exported Start trigger, Exported Script trigger, Ready for Start event, Started event, or Done event
Output impedance	

Main Path	50 Ω , nominal
Direct Path	50 Ω (+4%, –0%)
Maximum Output Overload	–2 V to +6.5 V
Output voltage	
Minimum V_{OH}	
Open load	2.4 V
50 Ω load	1.3 V
Maximum V_{OL}	
Open load	0.4 V
50 Ω load	0.2 V
Rise/Fall Time	3 ns typical.

Triggers and Events

Triggers

Sources	PFI<0..1> (SMB front panel connectors), PXI_Trig<0..7> (backplane connector), or Immediate (does not wait for a trigger). Immediate is the default value.
Types	Start trigger edge, Script trigger edge and level, and software trigger
Edge detection	Rising, falling

Minimum Pulse Width	25 ns
Delay from Trigger to Analog Output with OSP Disabled	154 Sample clock timebase periods + 65 ns, nominal
Additional Delay with OSP Enabled	Varies with OSP configuration.
Trigger exporting	
Exported Trigger Destinations	PFI<0..1> (SMB front panel connectors) or PXI_Trig<0..6> (backplane connector)
Exported Trigger Delay	50 ns, nominal
Exported Trigger Pulse Width	>150 ns

Events

Destinations	PFI<0..1> (SMB front panel connectors) or PXI_Trig<0..6> (backplane connector)
Types	Marker<0..3>, Data Marker<0..1>, Ready for Start, Started, Done
Quantum	Marker position must be placed at an integer multiple of two samples. There are two data markers per channel.
Width	Adjustable, minimum of 2 samples. Default is 150 ns.
Skew, with respect to analog output	
PFI<0..1>	±3 Sample clock periods

PXI_Trig<0..6>	±6 Sample clock periods

Waveform Generation Capabilities

Memory Usage	The PXIe-5451 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.
Onboard Memory Size	
128 MB option	134,217,728 bytes
512 MB option	536,870,912 bytes
2 GB option	2,147,483,648 bytes
Loop Count	1 to 16,777,215; Burst trigger: Unlimited
Quantum	Waveform size must be an integer multiple of two samples.
Output modes	Arbitrary Waveform, Script, and Arbitrary Sequence

Table 19. Minimum Waveform Size (Samples)

Trigger Mode	Number of Channels	Arbitrary Waveform Mode	Arbitrary Sequence Mode >180 MS/s	Arbitrary Sequence Mode ≤180MS/s
Single	1	4	2	2
	2	4	4	4

Trigger Mode	Number of Channels	Arbitrary Waveform Mode	Arbitrary Sequence Mode >180 MS/s	Arbitrary Sequence Mode ≤180MS/s
Continuous	1	142	140	58
	2	284	280	116
Stepped	1	210	154	54
	2	420	308	108
Burst	1	142	1,134	476
	2	284	2,312	952

Table 20. Memory Limits (Bytes)

Generation Mode	Number of Channels	128 MB	512 MB	2 GB
Arbitrary Waveform Mode, Maximum Waveform Memory	1	67,108,352	268,434,944	1,073,741,312
	2	33,553,920	134,217,216	536,870,400
Arbitrary Sequence Mode, Maximum Waveform Memory	1	67,108,352	268,434,944	1,073,741,312
	2	33,553,920	134,217,216	536,870,400
Arbitrary Sequence Mode, Maximum Waveforms	1	1,048,575	4,194,303	16,777,217
	2	524,287	2,097,151	8,388,607
Arbitrary Sequence Mode, Maximum Segments in a Sequence	1	8,388,597	33,554,421	134,217,717
	2	4,194,293	16,777,205	67,108,853

Table 21. Maximum Waveform Play Times

Sample Rate	Number of Channels	128 MB	512 MB	2 GB
400 MS/s	1	0.17 seconds	0.67 seconds	2.68 seconds
	2	0.084 seconds	0.34 seconds	1.34 seconds
25 MS/s	1	2.68 seconds	10.74 seconds	42.95 seconds
	2	1.34 seconds	5.37 seconds	21.47 seconds
100 kS/s	1	11 minutes 11 seconds	44 minutes 44 seconds	2 hours 58 minutes 57 seconds
	2	5 minutes 35 seconds	22 minutes 22 seconds	1 hour 29 minutes 29 seconds

Onboard Signal Processing

I/Q Rate

OSP Interpolation Range	2, 4, 8, 12, 16, 20 24 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16) 16,384 to 32,768 (multiples of 32)
I/Q Rate	Sample clock rate ÷ OSP interpolation
Data Processing Modes	Real (I path only) or Complex (I/Q)
OSP Modes	IF or Baseband
Maximum Bandwidth	0.8 × I/Q rate. When using an external I/Q modulator, RF Bandwidth = 0.8 × I/Q rate.

Prefilter Gain and Offset

Prefilter Gain and Offset Resolution	21 bits
Prefilter Gain Range	−16.0 to +16.0 (|Values| < 1 attenuate user data)
Prefilter Offset Range	−1.0 to +1.0
Prefilter Output	(User data × Prefilter gain) + Prefilter offset

Finite Impulse Response (FIR) Filtering

Table 22. FIR Parameters by Filter Type

Filter Types	Parameter	Minimum	Maximum
Flat	Passband	0.4	0.4
Raised cosine	Alpha	0.1	0.4
Root raised cosine	Alpha	0.1	0.4

Numerically Controlled Oscillator (NCO)

Maximum Frequency	0.4 * **sample rate**
Frequency Resolution	**Sample rate**/2
Tuning Speed	250 µs, typical

Digital Performance

Maximum NCO Spur	<-90 dBc
Interpolating Flat Filter Passband Ripple	<0.1 dB

Interpolating Flat Filter Out-of-Band Suppression	>80 dB

IF Modulation Performance

Table 23. IF Modulation Performance, Nominal

QAM Order	Symbol Rate (MS/s)	Alpha	Bandwidth	EVM (%)			MER (dB)		
				40 MHz IF	70 MHz IF	110 MHz IF	40 MHz IF	70 MHz IF	110 MHz IF
M = 4	0.16	0.25	200 kHz	0.2	0.2	0.2	57	57	56
	0.80	0.25	1.00 MHz	0.2	0.2	0.2	57	56	55
	4.09	0.22	4.98 MHz	0.2	0.3	0.2	57	52	55
M = 16	17.6	0.25	22.0 MHz	0.3	0.5	0.4	51	45	49
	32.0	0.25	40.0 MHz	0.6	—	0.6	42	—	43
M = 64	5.36	0.15	6.16 MHz	0.2	0.3	0.2	54	51	53
	6.95	0.15	7.99 MHz	0.3	0.3	0.3	52	51	50
	25.0	0.15	28.75 MHz	0.4	0.6	0.4	46	43	46
M = 256	6.95	0.15	7.99 MHz	0.3	0.3	0.4	52	51	49

Calibration

External Calibration	The external calibration calibrates the ADC voltage reference and passband flatness. Appropriate constants are stored in nonvolatile memory.

Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. Onboard channel alignment circuitry is used to calibrate the skew between channels. The self-calibration is initiated by the user through the software and takes approximately 60 seconds to complete. Appropriate constants are stored in nonvolatile memory.
Calibration Interval	Specifications valid within 1 year of external calibration
Warm-up Time	15 minutes

Power

+3.3 VDC	
Typical	1.9 A
Maximum	2.0 A
+12 VDC	
Typical	2.6 A
Maximum	2.9 A
Total power	
Typical	37.5 W
Maximum	41.4 W

Physical

Dimensions	3U, two-slot, PXI Express module 21.6 cm × 4.0 cm × 13.0 cm (8.5 in. × 1.6 in. × 5.1 in.)
Weight	550 g (19.4 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-25 °C to 85 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions

- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

> **Note** In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

> **Note** Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

> **Note** For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)