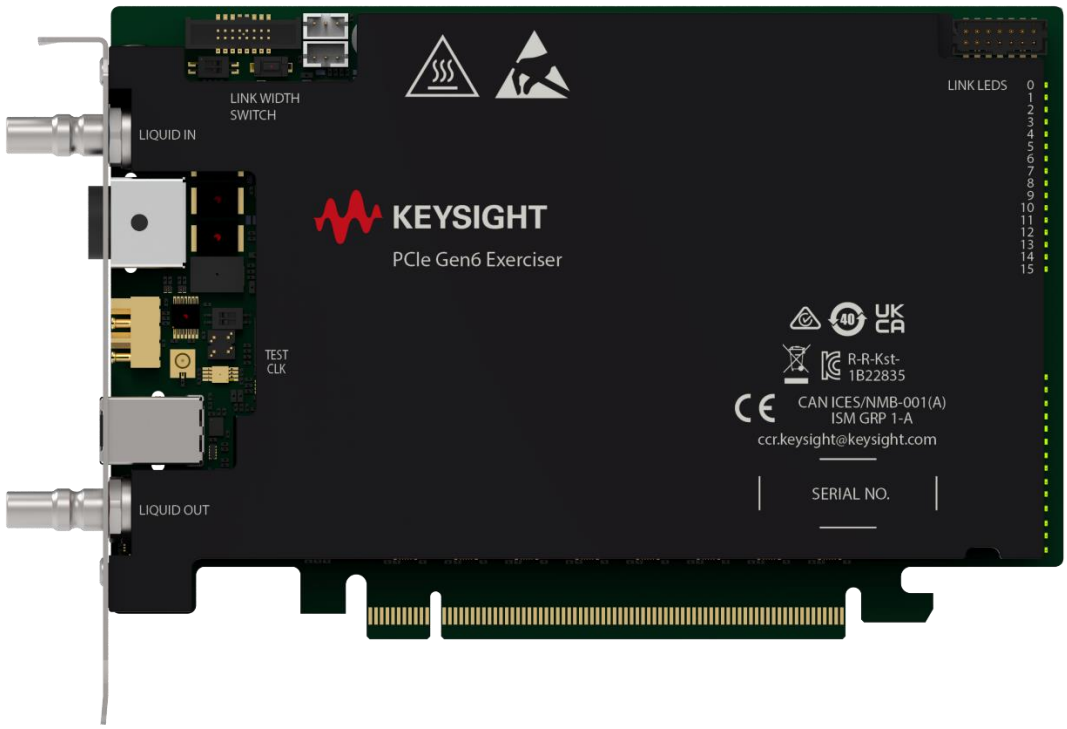
P5573A

PCI Express® Protocol Exerciser for PCIe® 6.0

Introduction

P5573A PCIe 6.0 Protocol Exerciser allows test engineers to emulate both PCIe root complex and endpoint devices when validating PCIe designs. The exerciser supports traffic generation from 2.5 GT/s through 64 GT/s and lane widths from x1 to x16. The tool includes over 100 built-in LTSSM test cases, error insertion capability at the TLP and DLLP layer, and an included protocol checker.



KEYSIGHT

Product Overview

The Keysight P5573A PCIe 6.0 Protocol Exerciser provides test and validation engineers a powerful tool for vetting and debugging their PCIe designs. The P5573A uses an integrated, single add-in-card design which greatly simplifies the connection and setup of the tool while offering greatly improved signal integrity compared to other architectures. This enables test and validation engineers to focus their time and energy on designing and automating unique test cases for their products, rather than wasting time dealing with an overly complex test setup with poor signal integrity.

The foundation of the P5573A is the improved signal integrity provided through the integrated design of the Exerciser card which provides a solid, trustworthy test platform. This compact design allows Keysight engineers great versatility in ensuring that the P5573A would have signal integrity characteristics that could be configurable enough to be tuned for many different test environments, while also offering quick link up capability for test cases that focus on higher layer protocol debugging.

The P5573A Exerciser supports PCIe speeds from 2.5 GT/s up to 64 GT/s lane widths up to x16 (P5573A), x8 (P5574A) and x4 (P5575A) along with the following features:

- Automated link training to 64GT/s
- Ability to initiate Higher and Lower Speed Changes between 2.5GT/s to max supported speed.
- PCIe 6.0 link training bypass
- Traffic generation directly from GUI or from automated user generated scripts.
- Lane Reversal and polarity detection
- Scalable flow control supported
- Control of the Link Training and Status State Machine (LTSSM) operation
- Lane and Speed Negotiations from 2.5 GT/s to 64 GT/s.
- Real Time Equalization process
- Transaction Layer Generation (Memory Read/Write, IO Request, Config Request)
- Emulate either upstream (Root Complex) or downstream (Endpoint) ports

Combined Exerciser and Analyzer Software

Both the Keysight P5573A PCIe 6.0 Protocol Exerciser and its companion tools, the P5570A P5570A/P5571A/P5572A PCIe 6.0 Analyzers, are supported by a single combined software interface, offering the user easy access to all of the powerful capabilities of both tools. Through a simple, tab based interface, the user can configure the Exerciser and Analyzer side by side with just a few clicks. The Exerciser GUI provides deep functionality for configuring Traffic Setup, while also providing improved data exchange with the analyzer.

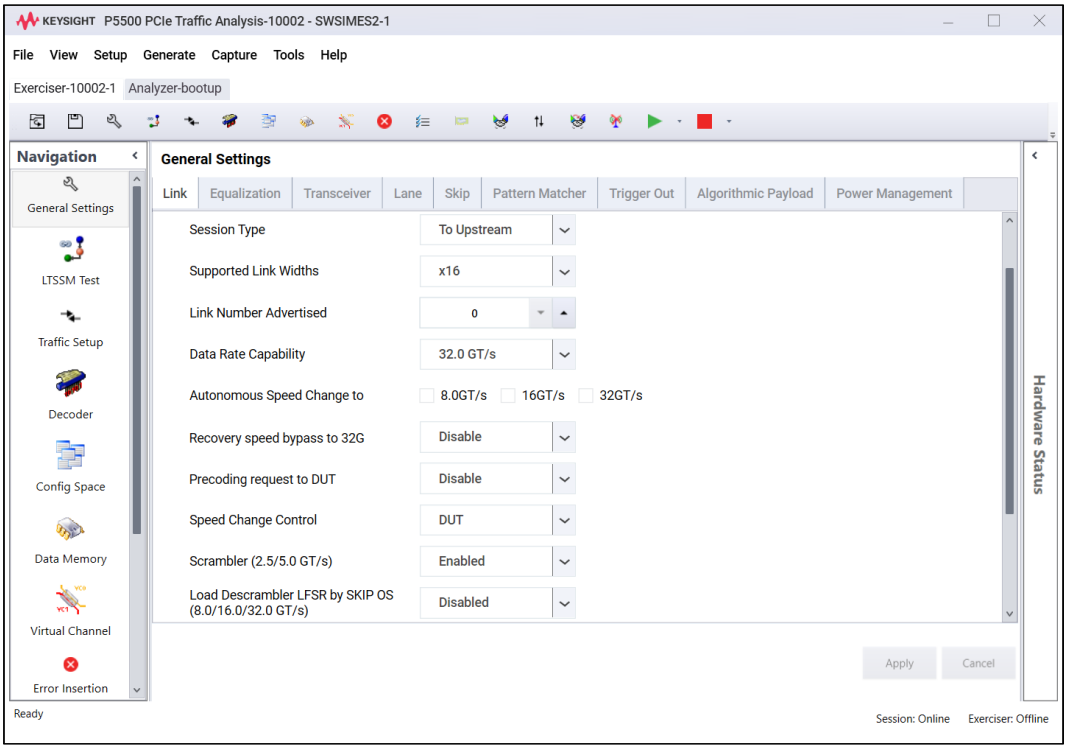


Figure 1. Exerciser equalization configuration.

Backplane Test Platform

Even more test setups can be created using the P5573A Exerciser along with the Keysight P5563B PCIe 6.0 Protocol Backplane Test Platform. The P5563B Test Platform features SI enhancements to reduce crosstalk and improve signal integrity, where low-loss material in utilized in order to support reliable connections at 64 GT/s.

- CEM form factor for endpoint devices. Automated link training to 64 GT/s
- Integrated low noise power supply with Auxiliary PCIe power available for high power endpoint devices
- Stable mechanical construction for reliable operation during bring-up
- One pair of CEM slots for connecting the Exerciser with a DUT.

Figure 2. P5563B Test Backplane

Use Case: Root Complex Emulation for Testing Endpoints

The Keysight P5573A can be configured to emulate a PCIe 6.0 root complex with its own link, equalization, and power management parameters.

When emulating a root complex, the P5573A cards can connect to a PCIe slot on the P5563B test backplane board with an endpoint (DUT) sitting in another PCIe slot. The exerciser then provides downstream stimulus to the DUT as a root complex just as a regular Host System would. The exerciser then can check the data received from the DUT for errors. This common configuration is simple to setup and easy for the end user to operate and troubleshoot.

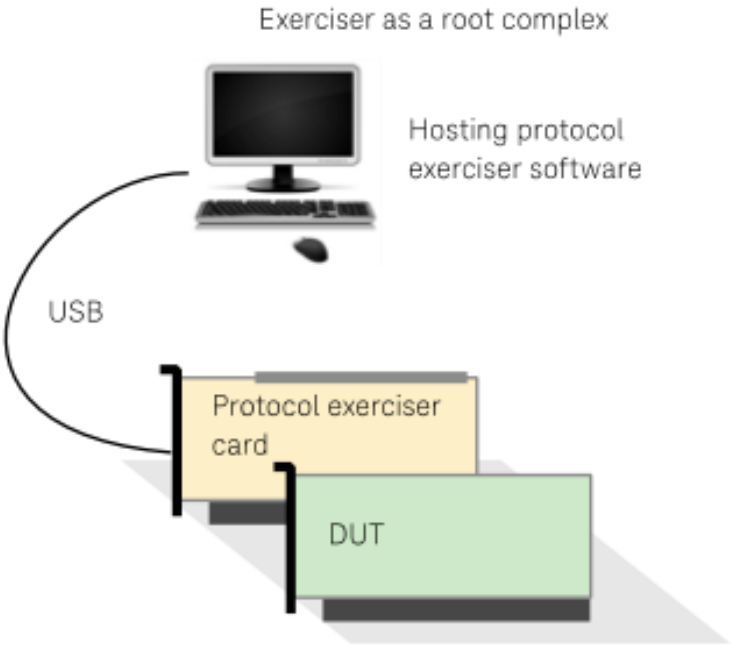


Figure 3. The P5573A PCIe 6.0 Protocol exerciser can be used to emulate a root complex.

The P5570A/P5571A/P5572A PCIe 6.0 Protocol Analyzer can also be added to the above configuration to decode and analyze the traffic between the emulated root complex and end point DUT.

Use Case: PCIe End Point Emulation for Testing Root Complex

When emulating an end point the PCIe exerciser card can be plugged into any PCIe slot on a system motherboard, similar to how any other PCIe add-in-card device, such as a NIC, Graphics Card, or SSD, would be plugged in.

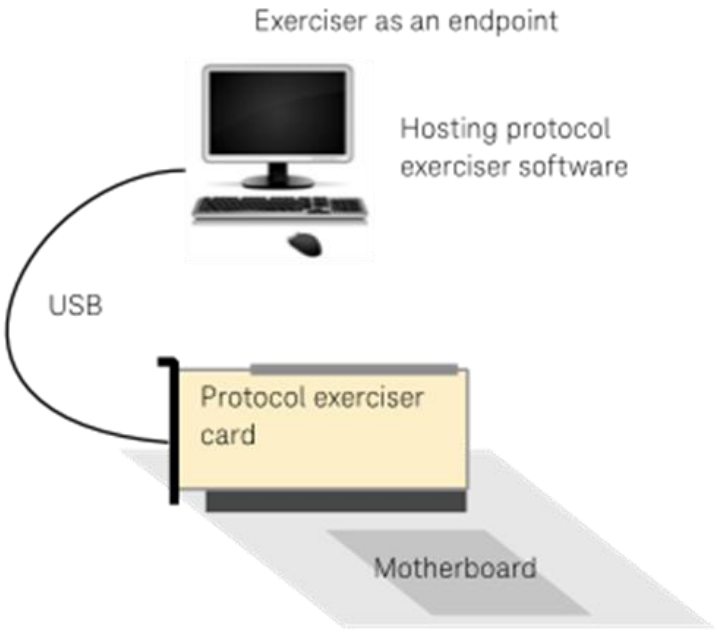


Figure 4. The P5573A PCIe 6.0 Protocol exerciser can be used to emulate a PCIe endpoint.

The P5573A PCIe 6.0 Protocol Analyzer can also be added to the above configuration to decode and analyze the traffic between the system motherboard and the emulated end point.

Ready to Go Protocol Test Features

The P5573A is designed to be easy to setup, connect, and be quickly configured to bring up the PCIe link and check basic LTSSM and protocol functionality. To support this the P5573A has many features included that allow for quick validation of fundamental PCIe features.

LTSSM Tester

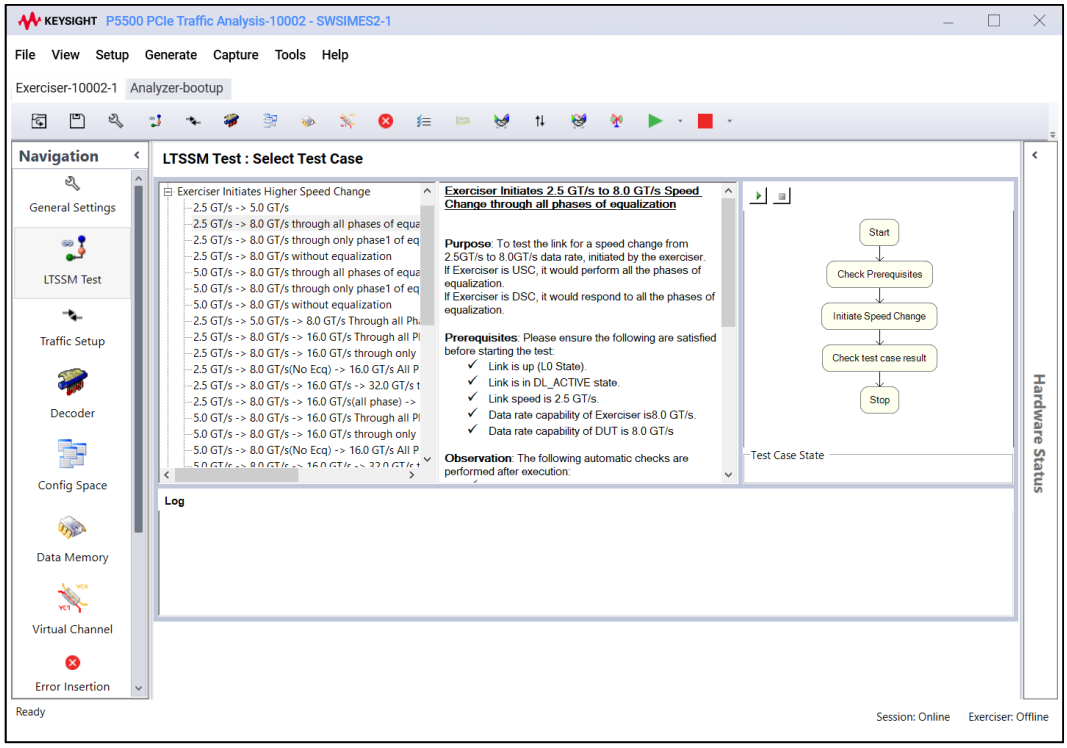


Figure 5. Over 100 LTSSM test cases are included.

LTSSM Tester mode allows the user to validate the different paths through the branches of the Link Training Sequence State Machine that are defined for PCIe.

Link Configuration

The P5573A PCIe 6.0 Exerciser supports a wide variety of configuration options for the PCIe link providing the user with a powerful tool for testing PCIe devices. The user has the ability configure the following parameters:

- Emulate upstream or downstream portLane widths of x1, x2, x4, x8 (P5574 only) up to 64 GT/s
- Data Rate support for 2.5 GT/s, 5 GT/s, 8 GT/s 16 GTs, 32 GT/s, 64GT/s
- Autonomous Speed Change capability for 8 GT/s 16 GTs, 32 GT/s, 64GT/s

Lane Configuration

The P5573A PCIe 6.0 Exerciser supports automatic lane reversal to be enabled and disabled, as well as the ability to invert transmitter lane polarity on specific lanes.

Equalization and Transceiver Configuration

The P5573A PCIe 6.0 Exerciser provides several options for controlling Link Equalization parameters which enable the user to create specific scenarios for testing link bring up. For 8 GT/s, 16GT/s, 32 GT/s and 64GT/s the user can both specify parameters for the Exerciser to use and configure the Exerciser to make certain Equalization requests to the DUT such as:

- PCIe transmitter equalization preset.
- Apply specific presets to individual lanes at certain speeds.

Automation API

Building customized test cases enables test engineers to fully vet the unique functionality of their products. Automating those test cases allows test engineers to accomplish more testing in less time, building confidence in the reliability of their designs. To enable this, the P5573A supports several scripting and automation capabilities that test engineers have asked for. The P5573A supports C# and Python APIs for scripting and automation.

Product Specifications

General characteristics	
Link widths	x1, x2, x4, x8, x16
Data rates	2.5 GT/s (PCIe 1.0), 5.0 GT/s (PCIe 2.0), 8.0 GT/s (PCIe 3.0), 16.0 GT/s (PCIe 4.0), 32 GT/s (PCIe 5.0) and 64GT/s (PCIe 6.0)
Speed	32 GBaud NRZ and PAM4 per lane
Clocking architecture	Common Clock architecture
Physical characteristics	
Size	(Standard height) half-length PCIe module 106.7 mm (4.2 inches) high and 167.65 mm (6.6 inches) long
Weight	408 gr (0.9 lb) Shipping weight: 2.36 Kg (5.2 lb)
Connectors	Power input, USB 3.0, and two mini-coax connectors for trigger in and out. Edge connector width is determined by the Link Width configuration purchased. Note: The edge connector is not upgradable after purchase and Keysight does not recommend or support the use of lane adaptors as they have a negative impact on the unit's performance at high speeds.
Cover	The hardware board has a cover to provide rigidness to the board.

Power requirements

Input	12 Vdc, 14 A maximum
Maximum power requirement	180 W
Power dissipation	150 W maximum
Keysight part number 0950-6474 external power supply supplied with the Exerciser	
Input	100 to 240 V at 4.0 A maximum, 50 to 60 Hz

LTSSM unsupported states

The Keysight P5573A supports all of the LTSSM states except the following unsupported states:

- L2
- Loopback

P5573A trigger specifications

Trigger output	
Output impedance	50 ohms
Threshold voltage	VOH - 2.4 V VOL – 0.55 V
Amplitude	2.4 V into open, 1.2 V into 50 ohms
Pulse width	120 nS
Trigger input	
Maximum input	3.0 V
Threshold voltage (VIH)	2.0 V

Environmental specifications

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment.	
Temperature	Operating: +5 °C to +35 °C Storage: -40 °C to +70 °C
Humidity	Operating: 15 to 85% (relative humidity, non-condensing) Storage: 15 to 95% (relative humidity, non-condensing)
Altitude	2000 m (6,500 feet) maximum
EMC and safety	IEC 61326-1 IEC 61010-1 / EN 61010-1 Canada: CSA C22.2 No. 61010-1 USA: UL 61010-1

Additional Recommended Hardware

While the Keysight P5573A PCIe 5.0 Protocol Exerciser is quite versatile as a stand alone test tool, more complicated test configurations can be supported when the P5573A is paired with additional Keysight hardware to improve analysis capability, robustness, and mechanical stability. Additional Keysight products that support the P5573A are shown below.

Description	Keysight model number(s)	Comments
PCIe 6.0 Protocol Analyzer	P5570A/P5571A/P5573A	
PCIe 6.0 Test System (backplane)	P5563B	

Ordering Information

Model	Description	Comments
P5575A	PCIe 6.0 Exerciser Linkwidth x4	
P5574A	PCIe 6.0 Exerciser Linkwidth x8	
P5573A	PCIe 6.0 Exerciser Linkwidth x16	
P5577PSWA	PCIe 6.0 Exerciser Software	Required for use of Exerciser
P5572A	PCIe 6.0 Analyzer Linkwidth x4	
P5571A	PCIe 6.0 Analyzer Linkwidth x8	
P5570A	PCIe 6.0 Analyzer Linkwidth x16	
P5576PSWA	PCIe 6.0 Analyzer Software	Required for use of Analyzer
R-55A-001-3	KeysightCare Assured - Extend to 3 years	
P5563B	PCIe 6.0 Test System (backplane)	

Software Licensing and KeysightCare Software Support Subscriptions

Keysight offers a variety of licensing options to fit your needs and budget. Choose your license term, license type, and KeysightCare software support subscription.

KeysightCare software support subscriptions

Perpetual licenses are sold with a 12 (default), 24, 36, or 60-month software support subscription. Support subscriptions can be renewed for a fee after that.

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KeysightCare Software Support Subscription provides peace of mind amid evolving technologies.

- Ensure your software is always current with the latest enhancements and measurement standards.
- Gain additional insight into your problems with live access to our team of technical experts.
- Stay on schedule with fast turnaround times and priority escalations when you need support.