

## **HSM Series**

### **RF SYNTHESIZER MODULES**

**Models in the range 12 GHz to 18 GHz**

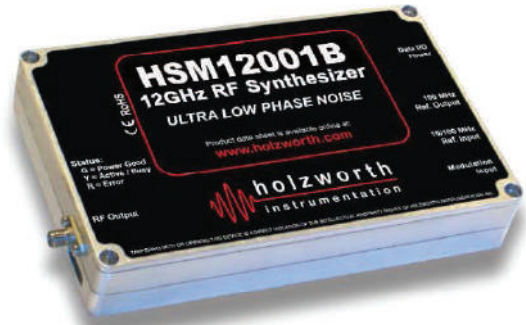


The Holzworth HSM Series RF Synthesizer Modules are stand alone, CW sources. These sources are designed as building blocks for systems integration where performance at the foundation is critical. Holzworth synthesizers provide incredible signal stability. The family includes modules spanning from 100 MHz to **12 GHz and 18 GHz**. When integrated as multiple units connected to the same reference signal, a phase coherent relationship is created which provides optimal unit-to-unit stability. 1 GHz, 2 GHz, 3 GHz, 4 GHz, and 6 GHz modules are also available. Details of these modules are included in a separate datasheet.

## HSM Series RF Synthesizers

### HYBRID ARCHITECTURE ENABLES BOTH LOW PHASE NOISE & FAST SWITCHING

The core architecture of the HSM Series modules is derived from Holzworth's proprietary NON-PLL design to provide the ultimate in phase / frequency stability. This direct-digital/direct-analog hybrid design was originally developed as a key building block for our phase noise analysis products. The hybrid architecture provides frequency agility & resolution, phase continuous switching and predictable performance without compromising on spurious or phase noise performance.



The attractive performance-to-price ratios available with the Holzworth HSM Series offer optimal solutions for electronics design, manufacturing test applications, and OEM systems integration.

### FREQUENCY OPTIONS

<b>HSM12001B</b>	12 GHz RF Synthesizer Module	100 MHz to 12.0 GHz	-110 dBc/Hz at 12 GHz (10 kHz offset)
<b>HSM18001B</b>	18 GHz RF Synthesizer Module	100 MHz to 18 GHz	-106 dBc/Hz at 18 GHz (10 kHz offset)

### DESIGN HIGHLIGHTS

- Agile Frequency Switching Speeds
- Pulse Modulation
- Onboard 100 MHz ULN OCXO
- 100 MHz Reference Out: -167 dBc/Hz (10 kHz OS)
- Reference Input: 10 MHz or 100 MHz
- SPI, USB, or Ethernet Communications Interface
- Internal Temperature Monitor Output

# HSM Series RF Synthesizers

## FREQUENCY PERFORMANCE

The specified frequency performance parameters for the HSM Series RF synthesizer modules are fully verified at final performance test and 100% guaranteed for the full warranty period of the product.

PARAMETER	MIN <sup>1</sup>	TYPICAL <sup>2</sup>	MAX <sup>1</sup>	COMMENTS
<b>Frequency Range</b>				
Model HSM12001B	100 MHz		12 GHz	VHF through X Band (settable from 10 MHz to 12.5 GHz)
Model HSM18001B	100 MHz		18 GHz	VHF through K <sub>u</sub> Band (settable from 10 MHz to 20.48 GHz)
<b>Frequency Step Size</b>		0.001 Hz		
<b>Phase Offset Range</b>	0 deg		+360 deg	
<b>Switching Speed (Frequency)</b>				No additional frequency settling time
SPI Mode (ASCII)		350 $\mu$ s		
SPI Mode (Binary)		200 $\mu$ s		
<b>Internal Time Base Reference</b>				
Adjust-to-Nominal			+/-0.2 ppm	Uncertainty
Aging Rate		$\pm 1$ ppm/yr		1 <sup>st</sup> year. $\pm 0.5$ ppm/yr each subsequent year
Temperature Effects		$\leq \pm 1$ ppm		0 to 55 °C
Line Effects		$\pm 0.1$ ppm		$\pm 5\%$
<b>Reference Output</b>				
Frequency		100 MHz		
Amplitude	+2 dBm		+6 dBm	Nominal
Impedance		50 $\Omega$		Nominal
<b>External Reference Input</b>				
Input Frequency		10 / 100 MHz		Software Select 10 MHz, 100 MHz or No Ext. Ref.
10 MHz Lock Range		$\pm 4$ ppm	$\pm 1$ ppm	20 Hz Locking BW, Internal OCXO remains on
10 MHz External Amplitude	0 dBm		+10 dBm	20 Hz Locking BW, Internal OCXO remains on, (nom)
100 MHz External	+2 dBm		+6 dBm	Internal OCXO shuts off, (nom)
Amplitude		50 $\Omega$		50 $\Omega$ (nom)
Impedance				Sine
Waveform				

<sup>1</sup> All MIN/ MAX performance parameters are guaranteed and 100% verified during final performance test, unless noted otherwise.

<sup>2</sup> Typical performance is "by design" and consistent with field performance data

# HSM Series RF Synthesizers

## AMPLITUDE PERFORMANCE

The specified amplitude based parameters for the HSM Series RF synthesizer modules are fully verified at final performance test and 100% guaranteed for the full warranty period of the product.

PARAMETER	MIN <sup>1</sup>	TYPICAL <sup>2</sup>	MAX <sup>1</sup>	COMMENTS
<b>Output Power (Calibrated)</b>				Settable -30 to +23 dBm
100 MHz to 10 GHz	-10 dBm		+18 dBm	
10 GHz to 18 GHz	-10 dBm		+16 dBm	
<b>Absolute Level Accuracy</b>				25 °C to 35 °C (case temperature)
100 MHz - 10 GHz				
-10 dBm to 0 dBm			± 3.0 dB	
> 0 dBm to < +14 dBm			± 1.5 dB	
+14 dBm to +18 dBm			± 2.0 dB	
10 GHz - 18 GHz				
-10 dBm to 0 dBm			± 3.0 dB	
> 0 dBm to < +10 dBm			± 1.5 dB	
+10 dBm to +18 dBm			± 2.5 dB	
<b>Resolution</b>		0.01 dB		
<b>Connector</b>		50 Ω		SMA
<b>VSWR (S<sub>22</sub>)</b>				
100 MHz ≤ f ≤ 6 GHz		1.33 (-17.0 dB)		Measured
6 GHz < f ≤ 18 GHz		1.43 (-15.0 dB)		Measured
<b>Maximum Reverse Power</b>	*** Some applications may require reverse power protection.			
Max DC Voltage	25 V <sub>DC</sub> maximum by design.			
> 10 MHz	16 dBm max by design.			
<b>Switching Speed (Amplitude)</b>		200 μs		Settled within 10% of set value
SPI Mode (Binary)				
<b>SSB Phase Noise</b>				Refer to typical data: Page 6
2.0 GHz, 10 kHz offset	-125 dBc/Hz		≤ -119 dBc/Hz	
4.0 GHz, 10 kHz offset	-119 dBc/Hz		≤ -113 dBc/Hz	
8.0 GHz, 10 kHz offset	-113 dBc/Hz		≤ -107 dBc/Hz	
12.0 GHz, 10 kHz offset	-110 dBc/Hz		≤ -104 dBc/Hz	
18.0 GHz, 10 kHz offset	-106 dBc/Hz		≤ -100 dBc/Hz	
<b>Harmonics (CW mode)</b>	<b>(2<sup>nd</sup> / 3<sup>rd</sup>)</b>	<b>(2<sup>nd</sup> / 3<sup>rd</sup>)</b>		Refer to typical data: Page 7
500 MHz to 5 GHz	-30 / -50 dBc	-25 / -45 dBc		@ 0 dBm
>5 GHz to 10 GHz	-25 / -45 dBc	-20 / -40 dBc		@ 0 dBm
>10 GHz to 18 GHz	-20 / -40 dBc	-15 / -35 dBc		@ 0 dBm
				3rd Harmonic level, nominal only above 16 GHz
<b>Sub-Harmonics (CW mode)</b>	<b>(<sup>1</sup>/<sub>2</sub> / <sup>3</sup>/<sub>2</sub>)</b>	<b>(<sup>1</sup>/<sub>2</sub> / <sup>3</sup>/<sub>2</sub>)</b>		Refer to typical data: Page 7
100 MHz to 3 GHz	-60 / -55 dBc	-54 / -49 dBc		@ 0 dBm
>3 GHz to 13 GHz	-44 / -60 dBc	-38 / -54 dBc		@ 0 dBm
>13 GHz to 18 GHz	-40 / -48 dBc	-35 / -45 dBc		@ 0 dBm
<b>Non-Harmonics (CW mode)</b>				Refer to typical data: Page 8
100 MHz to 4 GHz	-65 dBc	-59 dBc		@ 0 dBm
>4 GHz to 8 GHz	-50 dBc	-44 dBc		@ 0 dBm
>8 GHz to 16 GHz	-40 dBc	-35 dBc		@ 0 dBm
>16 GHz to 18GHz	-35 dBc	-30 dBc		@ 0 dBm
<b>Jitter (RMS)</b>				
3 GHz		85 fs		5 kHz < BW < 20 MHz
6 GHz		89 fs		
18 GHz		130 fs		

<sup>1</sup> All MIN/ MAX performance parameters are guaranteed and 100% verified during final performance test, unless noted otherwise.

<sup>2</sup> Typical performance is "by design" and consistent with field performance data

# HSM Series RF Synthesizers

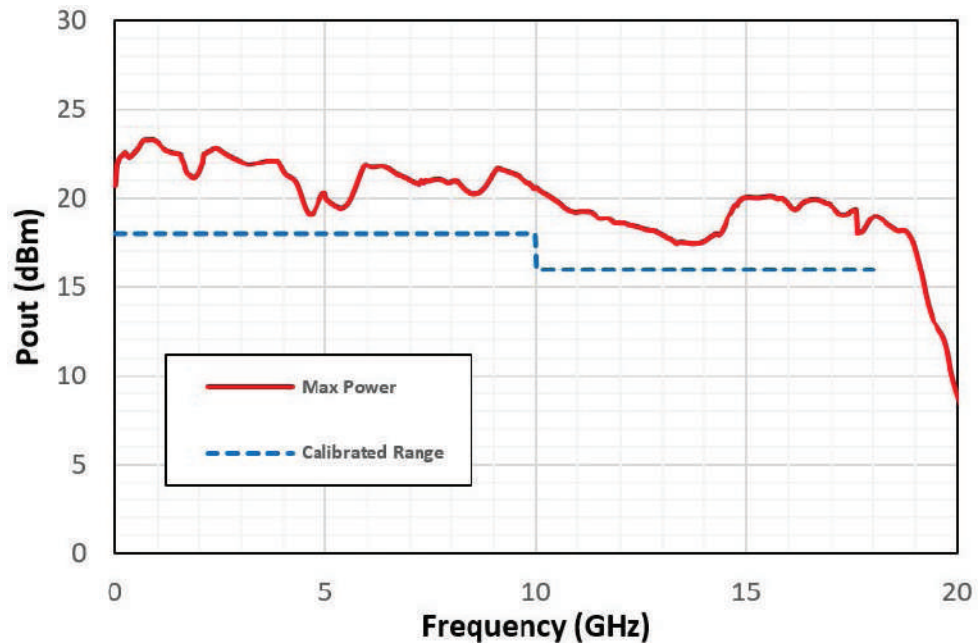
## OUTPUT POWER DATA

The data contained in this section demonstrates the typical output power performance of the HSM Series Designs.

### MAXIMUM AMPLITUDE THRESHOLD

Figure 1:

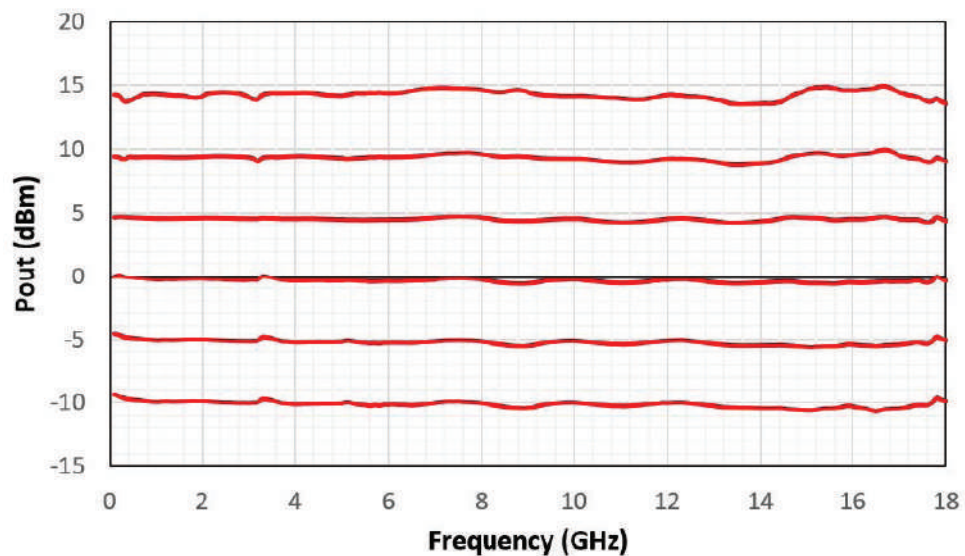
- Maximum Output Power
- +25 dBm Setting
- 10 MHz - 20 GHz



### CALIBRATED OUTPUT POWER

Figure 2:

- Calibrated Output Power
- -10 dBm to +15 dBm
- 100 MHz - 18 GHz

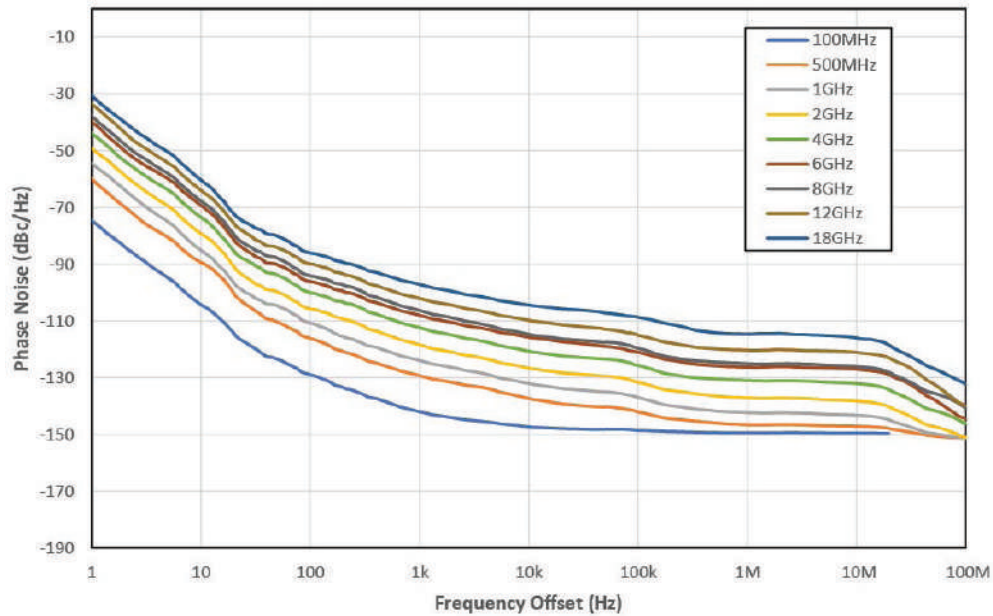


## HSM Series RF Synthesizers

### PHASE NOISE DATA

The raw data contained in this section demonstrates the typical phase noise performance of the HSM Series designs.

#### PHASE NOISE



**Figure 3:**

- Typical Phase Noise Performance Data
- 100 MHz - 18 GHz
- $P_{OUT}$  Setting: +10 dBm



# HSM Series RF Synthesizers

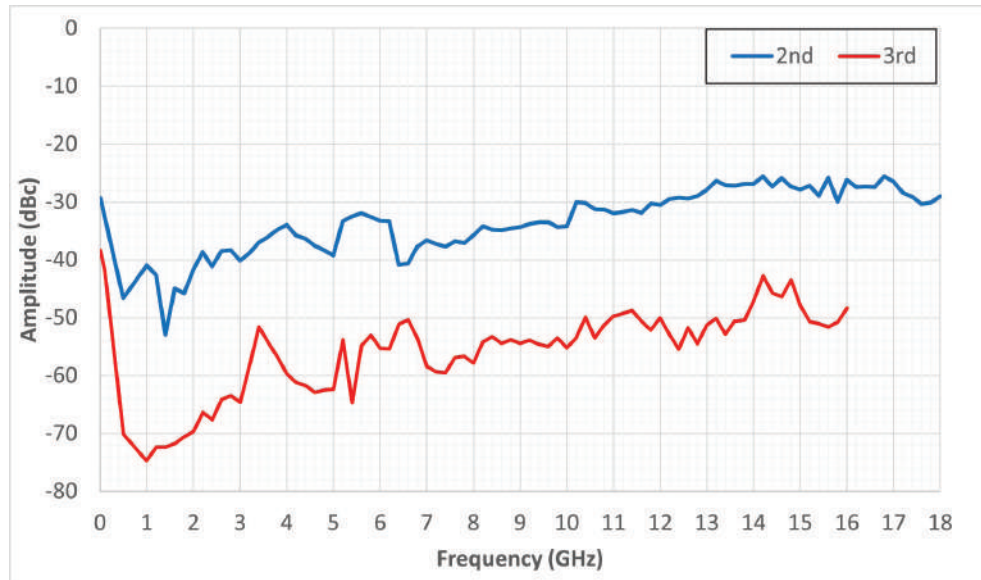
## SPECTRAL PURITY DATA

The data contained in this section demonstrates the typical spectral purity performance of the HSM Series designs.

### HARMONICS

**Figure 4:**

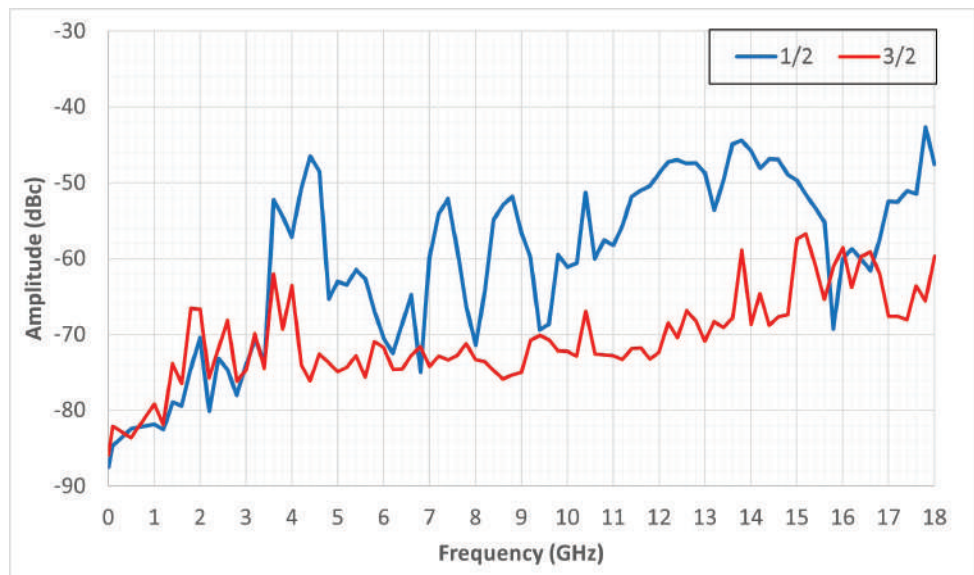
- Harmonics
- Typical Performance
- 10 MHz - 20 GHz
- P<sub>OUT</sub> Setting: +0 dBm



### SUB-HARMONICS

**Figure 5:**

- Sub-Harmonics
- Typical Performance
- 10 MHz - 20 GHz
- P<sub>OUT</sub> Setting: +0 dBm

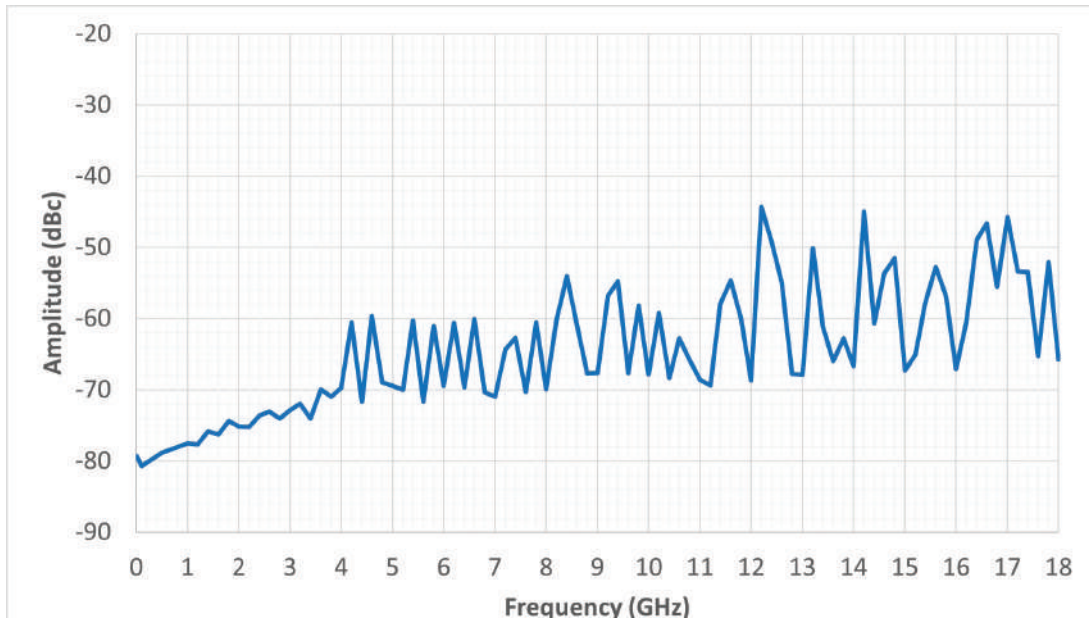


## HSM Series RF Synthesizers

### SPECTRAL PURITY DATA

The data contained in this section demonstrates the typical spurious performance of the HSM Series designs.

#### NON HARMONICS / BROADBAND SPURIOUS



**Figure 6:**

- Non-Harmonic Spurious, Typical Performance
- 10 MHz - 20 GHz
- $P_{OUT}$  Setting: +0 dBm
- Spectrum Analyzer Bandwidth Settings: 10 MHz Span, 10 kHz RBW, 10 kHz VBW



## HSM Series RF Synthesizers

### MODULATION PERFORMANCE (External Stimulus)

The modulation parameters listed here are based on modulation functions as related to the use of an external modulation stimulus.

PARAMETER	PERFORMANCE <sup>1</sup>	COMMENTS
<b>PULSE MODULATION (Analog)</b>		
<b>Risetime (Tr)</b>	<20 ns	
<b>Falltime (Tf)</b>	<20 ns	
<b>On/Off Ratio</b>		
100 MHz to 2 GHz	> 60 dB	
2 GHz to 5 GHz	> 50 dB	
5 GHz to 12 GHz	> 90 dB	
<b>Minimum Pulse Width</b>	<50 ns	
<b>ALC Loop Deviation (ALC disabled)</b>	1 dB difference from ALC enabled	

<sup>1</sup> Nominal

PARAMETER	PERFORMANCE <sup>1</sup>	COMMENTS
<b>External Trigger Threshold</b>	+1 V	±5% into 50 Ω

<sup>1</sup> Nominal

## HSM Series RF Synthesizers

### ENVIRONMENTAL SPECIFICATIONS

THIS MODULE IS DESIGNED FOR INDOOR USE ONLY

Environmental specifications are based on component margins, thermal verification testing and current draw tests.

PARAMETER	MIN <sup>1</sup>	TYPICAL <sup>2</sup>	MAX <sup>1</sup>	COMMENTS
Power Consumption <sup>3</sup>		15 W	18 W	18 W during warm-up
Operating Temperature	0 °C		+55 °C	

<sup>1</sup> All MIN/ MAX performance parameters are guaranteed and 100% verified during final performance test, unless noted otherwise.

<sup>2</sup> Typical performance is "by design" and consistent with field performance data

<sup>3</sup> See PINOUT CONFIGURATION tables on pages 15 and 16 for volt/amp ratings per pin.

#### REGULATORY COMPLIANCE

CE compliance with the following European Union directives  
Low Voltage Directive EU 2014/35  
Electromagnetic Compatibility Directive (EMC) EU 2014/30  
RoHS Directive EU 2015/863, WEEE Directive EU 2012/19

# HSM Series RF Synthesizers

## CONFIGURATION GUIDE

### STEP 1: SELECT MODULE FREQUENCY

FREQUENCY RANGE	MODEL NUMBER
100 MHz to 12 GHz	HSM12001B
100 MHz to 18 GHz	HSM18001B

### STEP 2: SELECT ADDITIONAL OPTIONS

The options listed in this section are available for the multi-channel platform to comply with application specific requirements.

OPTION	DESCRIPTION
SECURE	Secure option that wipes user settings when powered off. Model numbers ending in "S"

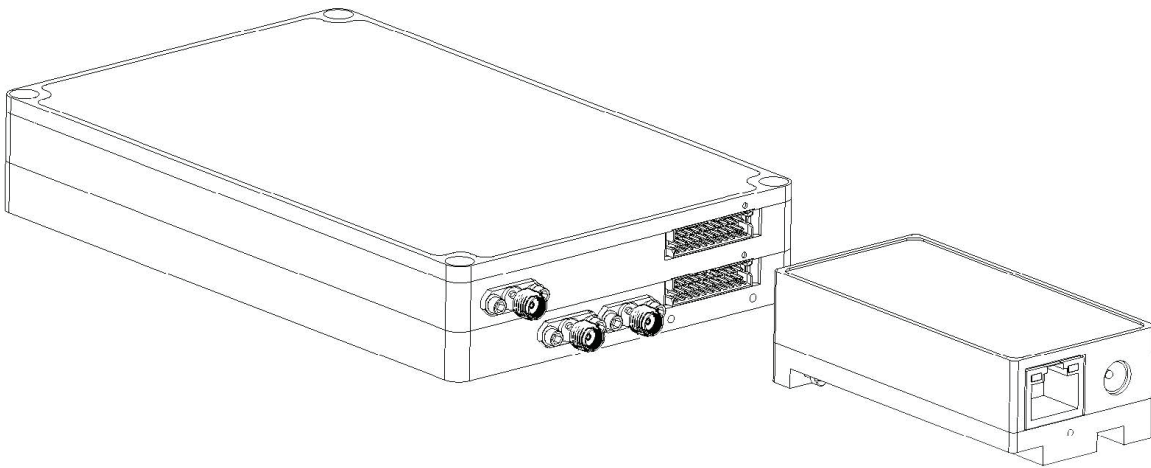
## HSM Series RF Synthesizers

### COMMUNICATION MODULES

Communications modules are also made available for ease of integration or simply to match legacy laboratory communications requirements. USB and Ethernet communication modules can be purchased from Holzworth directly.

#### HCM Communications Module Installation

The HCM Communication Module is an SPI to USB (or Ethernet) adapter that also includes a power supply adapter allowing the user to connect the RF synthesizer to standard AC power. The selected HCM Module creates a USB (or Ethernet) connection to a PC so that the Holzworth GUI, LabVIEW™, MATLAB™, etc. can be utilized to control the source. No drivers are required to run the Holzworth GUI.



**HCM6** USB Communications Module with power supply

**HCM7** Ethernet Communications Module with power supply

Each variation of the HCM Communications Module securely fastens to the synthesizer and comes complete with an AC power supply and the appropriate cable. HCM modules are a recommended accessory as the first step in integrating the HSM series synthesizers via the SPI bus. More information is available upon request.

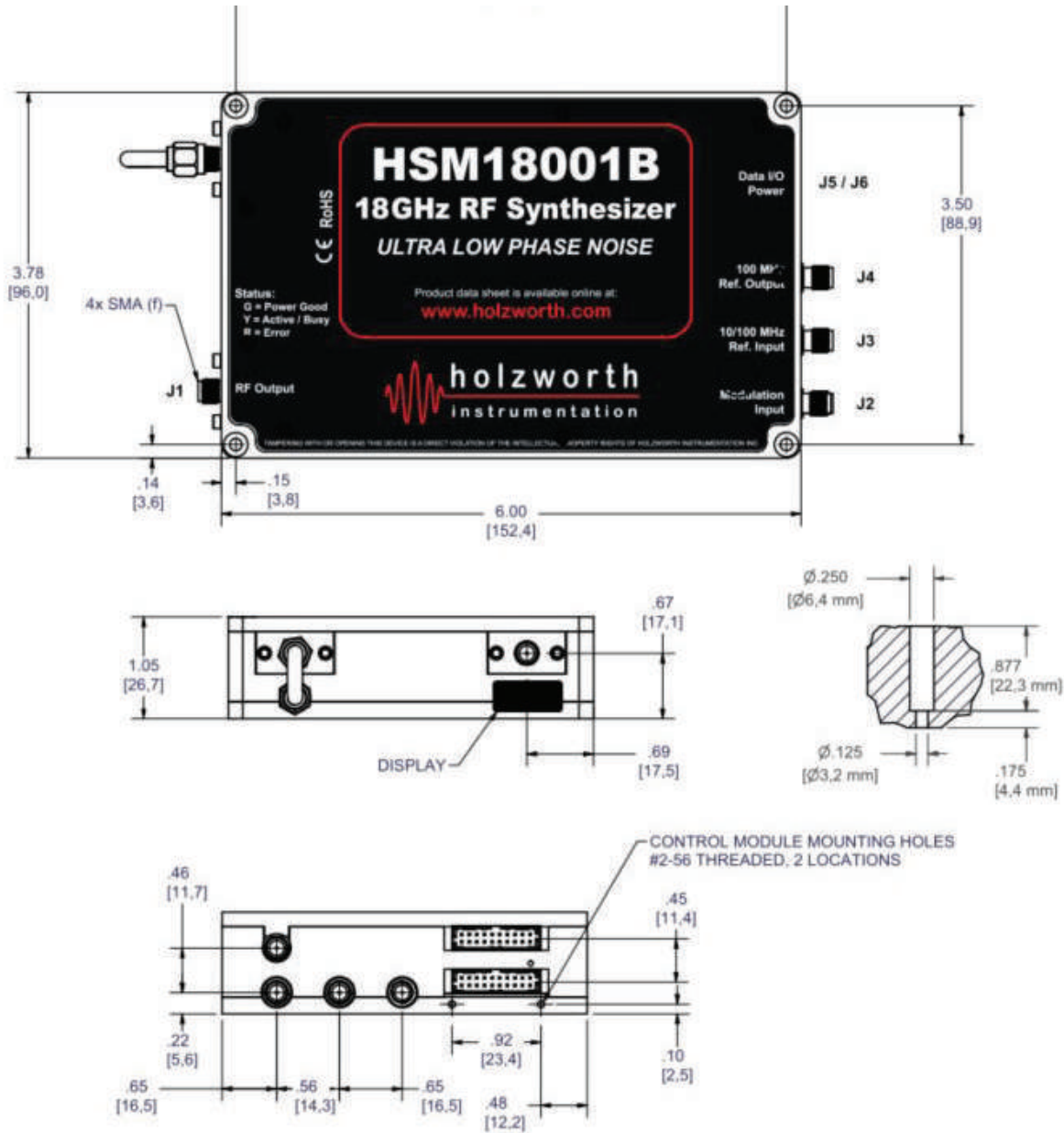
Do not exceed an ambient temperature of 45 °C when using an HCM module with the HSM.

If using a power supply, other than that provided with the HCM module use only an appropriately-rated, agency-approved power supply with +5 V DC and current rating of 5 A.

## HSM Series RF Synthesizers

### MECHANICAL CONFIGURATION

Mechanical details are in both inches and millimeters (listed inside parenthesis). All dimensions hold tolerances to within  $\pm 0.010$  inches.



# HSM Series RF Synthesizers

## INTERFACE DEFINITIONS

The interfaces defined within this section are cross referenced to the mechanical configuration included in this document. Ports are labeled on the synthesizer modules, but numbers are not physically printed on the module.

### J-PORT DEFINITIONS

PORT	DESCRIPTION	DESCRIPTION
<b>J1</b>	RF Output	SMA Jack
<b>J2</b>	Modulation Input	SMA Jack, Multiplexed, 50 ohm Input • Trigger/Pulse mod: 1.2 V Threshold
<b>J3</b>	10/100 MHz Ref. Input	SMA Jack: 10 MHz/100MHz Reference Input (software selectable)
<b>J4</b>	100 MHz Ref. Output	SMA Jack: 100 MHz Reference Output
<b>J5</b>	HSM <sup>1</sup> Data I/O - Power	2 mm, 20 pin (2x10) Milli-grid Shrouded Pin Header (detent type) Contains Power, Ground, SPI, and Status Indicators
<b>J6</b>	HSE <sup>1</sup> Data I/O - Power	2 mm, 20 pin (2x10) Milli-grid Shrouded Pin Header (detent type) Contains Power, Ground, SPI and Status Indicators
<b>Display</b>	Status	Tri-color LED Indicator Panel: GREEN = Power Good YELLOW = Communication Active / Busy / Not Ready RED = ERROR (i.e. no 10 MHz PLL lock, Unleveled, etc.)

### J5/J6 (SPI) MATING CONNECTOR PART NUMBERS

APPLICATION	MOLEX PART NUMER	DESCRIPTION
IDC Ribbon	Molex 87568-2093	2 mm Milli-Grid, 20 pin (2x10) Female, Polarization and Ramp Locking
Vertical PCB Thru Hole	Molex 79107-7009	2 mm Milli-Grid, 20 pin (2x10) Female, NO Polarization or Ramp Locking
Vertical PCB SMT	Molex 79109-1009	2 mm Milli-Grid, 20 pin (2x10) Female, NO Polarization or Ramp Locking

<sup>1</sup> HSM refers to the lower section of the synthesizer, while HSE refers to the high-frequency upconversion section. Each has a 20-pin connector.



# HSM Series RF Synthesizers

## J5 PINOUT CONFIGURATION

PIN No.	Label	PIN No.	Label
1	GND	2	GND
3	+ 5V, (1.5A Max)	4	+5V tied to pin 3
5	+12V , (600mA Max)	6	N.C. (reserved)
7	NC	8	N.C. (reserved)
9	/RESET (/RESET47k PU)	10	N.C. (reserved)
11	/CS (Module Select - 47k PU)	12	Trigger (5V Tolerant Input)
13	SDO (Synthesizer Data Output)	14	Power Good (OC – 47k PU to 3.3V)
15	SDI (Synthesizer Data Input)	16	/ERROR (OC – 47k PU to 3.3V)
17	SCLK (Synthesizer Clock Input)	18	/BUSY (OC – 47k PU to 3.3V)
19	GND	20	GND

## J5 PIN LABEL DEFINITIONS

PIN No.	Label
<b>+5V</b>	Nominally pulls 1.2A from the +5V Rail. Initially at power on the draw will be 100 mA then increase as subsystems power-on. Tolerance +8% to -1%. 4.95V to 5.4V.
<b>+12V [or +15V]</b>	Nominally 300 mA draw from this pin (T=25C). 600 mA draw at startup for at least 5 mins for OCXO power on. +15V O.K. but increases power dissipation.
<b>NC</b>	No Connect. Voltage supply pin. Not currently used.
<b>/RESET</b>	Active low on this pin put the module in reset, releasing it returns to reset operation. Module is ready 2-3 seconds after /RESET is released. 10K pullup to 3.3V in parallel to 0.01uF cap to ground.
<b>/CS</b>	Communications chip select, active low. 47K pullup on this line. /CS must be low for any communication to occur. Allows for multiple synthesizer modules on 1 SPI bus. 3.3V logic levels, 5V tolerant.
<b>SDO</b>	Synthesizer (module/slave) Data Output. Connects to Master Serial Data Input. Active when chip select is low. High-Z when /CS is high. 47K pulldown. 3.3V logic levels, 5V tolerant.
<b>SDI</b>	Synthesizer (module/slave) Data Input. Connects to Master Serial Data Output. High-Z input on module. 3.3V logic levels, 5V tolerant. 47K pulldown.
<b>SCLK</b>	SPI Clock (slave clock input). Idle Low, Active High. Data is transitioned into the module on a rising low to high transition. Data is transitioned out on the same edge and is valid on the falling edge of SCLK. 3.3V logic levels, 5V tolerant. 47K pulldown.
<b>TRIGGER</b>	CMOS Trigger input to the onboard microprocessor. 47k pulldown.
<b>Power Good</b>	Open collector output, 47k pullup to 3.3V. When high, power is healthy. When low, either voltages or currents are problematic. Module may not operate correctly. There is a 0.5 second delay from when power is applied to a valid PowerGood. Actual PowerGood may take up to 2 seconds to go high due to some very stable internal references that are settling. This may be multiplexed with other HSM6001 synthesizers.
<b>/ERROR</b>	Open collector output, 47k pullup to 3.3V. Nominally high. If an error condition occurs, such as a PLL unlock or un-leveled condition, this will go active low. This can be multiplexed with other HSM6001 synthesizers.
<b>READY or /BUSY</b>	Open collector output, 47k pullup to 3.3V. Nominally high. After an SPI communication, if a command has been issued, then the /BUSY will go active low until that command is finished. During this time no communication may occur and SPI bus will be asleep.

# HSM Series RF Synthesizers

## J6 PINOUT CONFIGURATION

PIN No.	Label	PIN No.	Label
1	GND	2	GND
3	+ 5V, (2A Max)	4	+5V tied to pin 3
5	+12V , (700mA Max)	6	N.C. (reserved)
7	-12V (50mA Max)	8	N.C. (reserved)
9	/RESET (10k PU)	10	N.C. (reserved)
11	/CS (Module Select - 47k PU) *	12	Trigger (5V Tolerant Input)
13	SDO (Synthesizer Data Output)	14	Power Good (OC – 47k PU to 3.3V)
15	SDI (Synthesizer Data Input)	16	/ERROR (OC – 47k PU to 3.3V)
17	SCLK (Synthesizer Clock Input)	18	/BUSY (OC – 47k PU to 3.3V)
19	GND	20	GND

## J6 PIN LABEL DEFINITIONS

PIN No.	Label
<b>+5V</b>	Nominally pulls 1.5A from the +5V Rail. Initially at power on the draw will be 100mA then increase as subsystems power-on. Tolerance +8% to -1%. 4.95V to 5.4V. The value supplied to the module can be checked via software.
<b>+12V [or +15V]</b>	±5%. Nominally 500mA from this pin (T=25C). The value supplied to the module can be checked via software.
<b>-12V</b>	±5%. Nominally 30mA from this pin (T=25C).
<b>/RESET</b>	Active low on this pin puts the module in reset, releasing it returns to reset operation. Module is ready 2-3 seconds after /RESET is released. 10K pullup to 3.3V in parallel to 10uF cap to ground.
<b>/CS</b>	Communications chip select, active low. 47K pullup on this line. /CS must be low for any communication to occur. Allows for multiple synthesizer modules on 1 SPI bus. 3.3V logic levels, 5V tolerant.
<b>SDO</b>	Master Serial Data Input (synthesizer module/slave data out). Active when chip select is low. High-Z when /CS is high. 47K pulldown. 3.3V logic levels, 5V tolerant.
<b>SDI</b>	Master Serial Data Output (synthesizer module/slave data in). High-Z input on module. 3.3V logic levels, 5V tolerant. 47K pulldown.
<b>SCLK</b>	SPI Clock (slave clock input). Idle Low, Active High. Data is transitioned into the module on a rising low to high transition. Data is transitioned out on the same edge and is valid on the falling edge of SCLK. 3.3V logic levels, 5V tolerant. 47K pulldown.
<b>TRIGGER</b>	CMOS Trigger input to the onboard microprocessor. 47k pulldown.
<b>Power Good</b>	Open collector output, 47k pullup to 3.3V. When high, power is healthy. When low, either voltages or currents are problematic. Module may not operate correctly. There is a 0.5 second delay from when power is applied to a valid PowerGood. Actual PowerGood may take up to 2 seconds to go high due to some very stable internal references that are settling. This may be multiplexed with other HSM series synthesizers.
<b>/ERROR</b>	Open collector output, 47k pullup to 3.3V. Nominally high. If an error condition occurs, such as a PLL unlock or un-leveled condition, this will go active low. This can be multiplexed with other HSM series synthesizers.
<b>READY or /BUSY</b>	Open collector output, 47k pullup to 3.3V. Nominally high. After an SPI communication, if a command has been issued, then the /BUSY will go active low until that command is finished. During this time no communication may occur and SPI bus will be asleep.
<b>N.C.</b>	These are reserved lines for use in our communications module. They should be left floating.

# HSM Series RF Synthesizers

## SPI COMMUNICATIONS

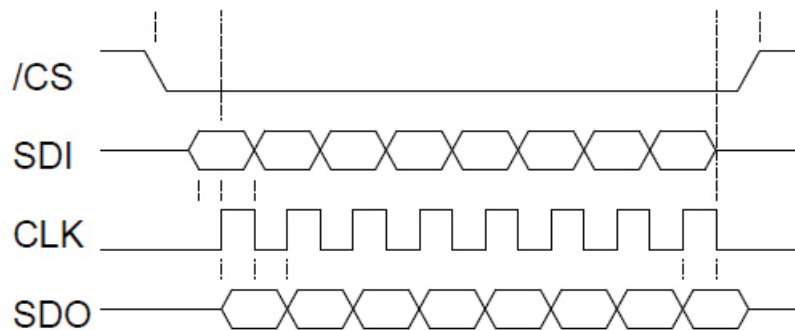
### BUS OVERVIEW

The SPI bus is a byte oriented bus, sending 8 bits at a time. Any number of bytes may be sent, from 1 byte to 64 bytes while chip select is low. Bytes sent beyond 64 bytes will be ignored. The data is held in a buffer until chip select goes high, initiating the parsing of the data and execution of the commands. The maximum speed of the bus is 10 Mbits/s. Data may be written to the module and data may be received from the module. After a command is sent requesting data, the next transfer sends this data out on SDO. During the read, a new command may be sent and will be parsed when chip select goes high. A read is always followed by a write with a read request.

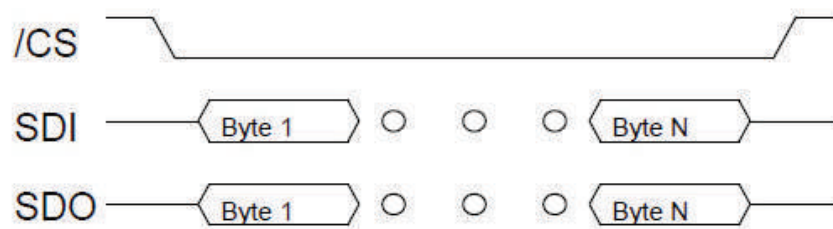
### BUS HARDWARE PROTOCOL

Data is clocked into the module on the rising edge of sclk. Data is clocked out of the module on this same edge. Data output is valid on the falling edge of sclk. Data is only transferred when chip select is low. When chip select goes high, this initiates the parsing and execution of data.

### SPI TIMING



The figure above demonstrates bit level timing where data is sampled into and out of the module on the rising edge of SCLK (Slave Clock). Data out is valid on the falling edge of SCLK.



The above figure displays how byte level communications occurs. Any number of bytes may be sent. After /CS goes high, the data is parsed and executed. If no data is sent, the SPI communications module simply resets itself and no parsing or execution of data occurs. If /CS goes high in the middle of a byte transfer (1-7 bits are sent instead of 8) this byte is ignored.

## **HSM Series** RF Synthesizers **WARRANTY**

All Holzworth HSM Series synthesizer modules come with a standard 3 year 100% product warranty covering manufacturing defects. All product repairs and maintenance must be performed by Holzworth Instrumentation. Holzworth reserves the right to invalidate the warranty for any products that have been tampered with or used improperly. Refer to Holzworth Terms & Conditions of Sales for more details.

**Holzworth products are proudly designed and assembled in the USA.**